NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

ALTERNATIVE GATE DESIGNS FOR IMPROVED RADIATION HARDNESS IN BULK CMOS INTEGRATED CIRCUITS

by

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March 1997

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REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE March 1997	3. REPORT TYPE AND DATES COVERED Master's Thesis

4. TITLE AND SUBTITLE
ALTERNATIVE GATE DESIGNS FOR IMPROVED RADIATION HARDNESS IN BULK CMOS INTEGRATED CIRCUITS

5. FUNDING NUMBERS

6. AUTHOR(S) Sidney Scott Noe

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Department of Defense
9800 Savage Road
Fort Meade, Maryland 20755-6000

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

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14. SUBJECT TERMS CMOS, radiation, hardening, integrated circuits, VLSI

15. NUMBER OF PAGES 249

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18 298-102

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ALTERNATIVE GATE DESIGNS FOR IMPROVED RADIATION HARDNESS IN BULK CMOS INTEGRATED CIRCUITS

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 1997

ABSTRACT

In the last 30 years, the world has become increasingly dependent on space-based systems. These systems require varying degrees of radiation tolerance to perform their missions. Current radiation hardening processes for integrated circuits are expensive and consume significant layout area, increase power consumption, and decrease the frequency of operation. Furthermore, it is becoming more difficult to find fabricators for radiation-hardened electronic devices. In this thesis, two new transistor designs using a bulk CMOS process are tested for radiation hardness and are compared to a standard design. Both show a degree of improvement in subthreshold leakage current and threshold voltage shift over the control transistors. The new designs demonstrate an ability to reduce the effects of radiation on transistor parameters by means of an applied voltage to a second layer of polysilicon material above the control gate material.

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ACKNOWLEDGMENT

The author would like to thank the National Security Agency for sponsoring this research and Dr. Gary Lum of Lockheed-Martin Missiles and Space for his assistance and the use of the lab facilities.

I. INTRODUCTION

The last decade has seen a dramatic increase in use of and dependence on space-based technology. The Department of Defense has placed an ever increasing demand on rapid information exchange systems for command, control, and communications, as well as overhead collection. Integrated circuits (ICs) are the critical components in these systems. The radiation environment in which these systems operate is responsible for over 4500 malfunctions in the last twenty five years [Ref. 1]. As ICs are made smaller and with higher performance capabilities, their susceptibility to certain radiation effects increases. Current efforts to improve the radiation tolerance of these devices are not keeping pace with other advances in microelectronics. Furthermore, current radiation-hardened ICs are often obsolete before they become available because of the time required to harden a commercial IC design.[Ref. 1 - 3]

While the United States has dominated the recent world market for radiation-hardened ICs by controlling approximately 60% of the market share, the end of the Cold War has signaled a drastic decline in Department of Defense demands. In an effort to decreased spending, the DoD is pushing for the use of Commercial-Off-the-Shelf (COTS) components.[Ref. 4 - 6] Correspondingly, DoD investment in radiation-tolerant microelectronics technology has dropped from $50 million to less than $20 million between 1989 and 1995. As a result, the number of available U.S. vendors for radiation hardened devices has dropped from twenty in 1990 to four in 1995.[Ref. 1]

In danger of losing its technical advantage and becoming dependent on foreign suppliers, the United States must find methods to maintain its production capability. In order to avoid the high cost of maintaining a radiation-hardened IC fabrication line, research is under way to fabricate radiation-tolerant ICs using a standard bulk CMOS process. If successful, the necessary devices could be produced using cheaper bulk CMOS processes and companies not in the rad-hard business could rapidly enter production should the need arise. The purpose of this thesis is to test some new experimental IC designs and evaluate their effectiveness at compensating for the change in threshold voltage and end-around gate leakage that usually occurs in field effect transistors at high total doses.

Chapter II of this thesis reviews the effects of radiation on ICs. Chapter III details the devices which were tested and the tests which were conducted. Two chips with three structures each were designed and fabricated. Each structure has three nMOS and three pMOS transistors. Chapter IV describes the testing that was performed and Chapter V presents the results. The final chapter draws conclusions as well as provide recommendations for further study.

II. RADIATION EFFECTS

The effects of radiation on integrated circuits are typically due to Total Dose Effects, Dose Rate Effects, and Single Event Effects (SEEs). These could result in the system providing false information or being rendered useless. Total dose effects are caused by long-term exposure to a radiation environment resulting in system degradation or complete failure. Dose rate and single event effects are similar. However, dose rate effects are caused by a large amount of radiation over a short time period and SEEs are caused by a single high-energy particle. Both can be categorized as either upsets or latch-up. An upset is a loss of data (a 1 changing to a 0 or a 0 to a 1). Latch-up refers to the turning on of parasitic circuits in CMOS devices. Once turned on, these parasitic circuits can quickly and permanently damage the device. Turning them off requires powering down the device.

A. IONIZING RADIATION

Ionizing radiation is composed of atomic particles. When these particles come in contact with a semiconductor device, a transfer of energy occurs. This energy causes the production of electron-hole pairs along the path of the ionizing particle. Some of these electron-hole pairs immediately recombine. Others migrate throughout the material leaving ionized atoms behind. This ionization can affect changes in the electrical characteristics of the device.[Ref. 7]

The effect on the device is both a function of dose and of dose rate. Ionizing dose is measured in radiation absorbed dose (rads). One rad is the dose depositing 100 ergs of energy per gram of material. Therefore it is necessary to specify the material. For integrated circuits, it is usually specified in rad (Si), rad (SiO_2) or rad (GaAs).[Ref. 7]

1. Ionization Particles

Space contains many high-energy atomic particles such as photons, protons, neutrons and electrons which can cause ionizing radiation damage. Celestial bodies like the sun and stars give off protons, electrons and heavy ions. These particles can also be produced by a nuclear detonation [Ref. 4, 8]. The South Atlantic Anomaly is an area of particularly high atomic particle density. It results from the fact that the earth's magnetic field is not centered on the earth's center and is not aligned with the equator [Ref. 2].

Two of the main ionization-causing particles are gamma and x-rays. Gamma rays and x-rays are high energy photons. They are waves of electromagnetic energy. As these particles penetrate a device, they give up their energy to the device material via the photoelectric effect, the Compton effect, or pair production, depending on the amount of energy the incident particle has. Ionization can also be caused by the collision of neutrons with the lattice atoms of the semiconductor. These atoms or molecules become displaced, resulting in a distortion of the device lattice structure. This is called displacement damage and it can degrade the conducting properties of the semiconductor material. Some of

these displaced atoms will take the places vacated by others. Some will combine with doping or impurity atoms to form stable defects. Mobile vacancies, however, can combine with these atoms and form recombination or trapping centers which will trap minority carriers and alter the characteristics of the device by reducing minority carrier lifetime and increasing conductivity.[Ref. 7]

2. Charge Trapping

Charge trapping is a major mechanism of change in MOS device characteristics. As the incident photons penetrate the SiO_2 insulator and electron-hole pairs are created, an electric field is generated. As previously stated, some of the electron-hole pairs immediately recombine. Those that do not are swept away by the electric field. The electrons, having a higher mobility than holes (>2.5 times), are swept out of the insulator while holes remain trapped because there are energy levels existing in the insulator to capture holes. For an nMOS device, these holes are normally repelled towards the channel, due to positive gate bias, and accumulate along the Si-SiO_2 interface. This can be seen in Figure 2.1. This accumulation of charge is greatly affected by the gate bias during irradiation. Recent studies by Fleetwood et al. show that these charges will anneal out in time [Ref. 5, 9 - 14]. However, if the device is not removed from the radiation environment, as would be the case for space applications, the devices will not have time to anneal. In high quality insulators, the recombination process could last for days. This could lead to permanent device degradation. 3.6 eV is the average energy to ionize an electron-hole pair in silicon and that the number of electron-hole pairs created per incident

rad absorbed is constant at 4.05×10^{13} pairs per cm^3 rad (Si) for silicon, independent of temperature. [Ref. 7]

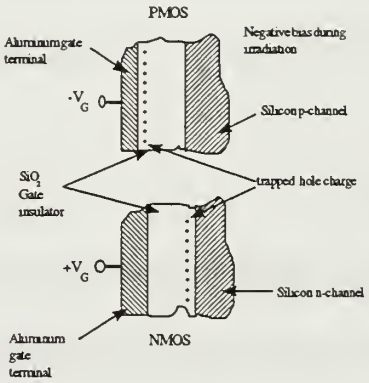


Figure 2. 1 Hole charge-trapping in gate insulators in enhancement mode MOS transistors after Ref. [7].

Post-irradiation characteristics are greatly affected by biasing voltages. A positive gate voltage with respect to the substrate will increase the charge separation within the oxide and push the holes closer to the Si-SiO_2 interface where they will have a greater effect on the charge carriers in the Silicon substrate [Ref. 4].

3. Total Dose Effects

In the radiation environment of space, the total ionizing dose is built up slowly over time with typical irradiation rates of 1 mrad (Si)/sec or less [Ref. 4]. Ionizing

radiation can cause voltage threshold shifts and increased leakage currents in CMOS devices [Ref. 2, 4, 7]. More information on this topic is located in references 5, and 9 through 22.

a. Threshold Voltage

The most significant effect of total dose ionization is a change in the threshold voltage of a device as a result of charge trapping. For an n-type device, the insulator already has a positive charge near the channel due to the trapped holes. The result is that less charge is required to turn the transistor on. Eventually, the device will be on permanently as the radiation drives the device toward depletion operation. In the pMOS transistor, the holes in the insulator migrate toward the gate electrode (negative bias) with the same result, a decrease in threshold voltage. This transistor then cannot be turned on as it is driven further into the enhancement region of operation. Figure 2.2 shows the effects of this phenomenon on the device I-V characteristics.

The threshold voltage shift is very dependent on the gate oxide thickness. The thinner the oxide, the shorter the distance holes must travel to exit the insulator and the fewer holes get trapped within the material [Ref. 8]. The large volume of a gate oxide increases the number of possible hole traps. Figure 2.3 shows the various threshold shifts for different oxide thicknesses. Current processes try to minimize the gate oxide thickness in order to improve the radiation tolerance of the device.

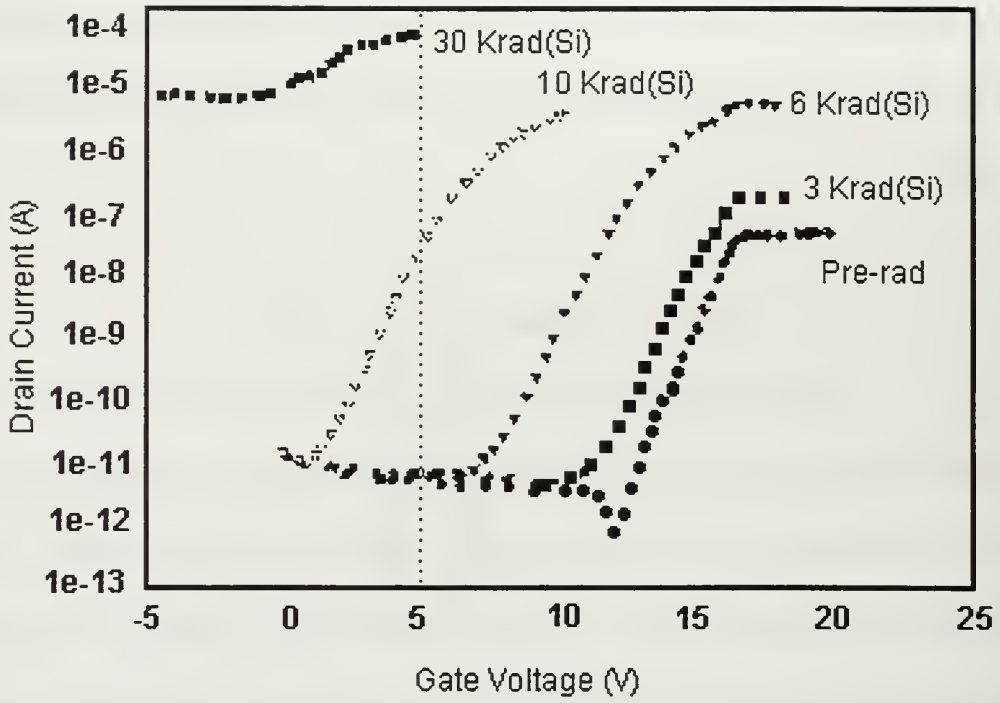


Figure 2.2. I-V Characteristics for a conventional nFET from Ref. [4].

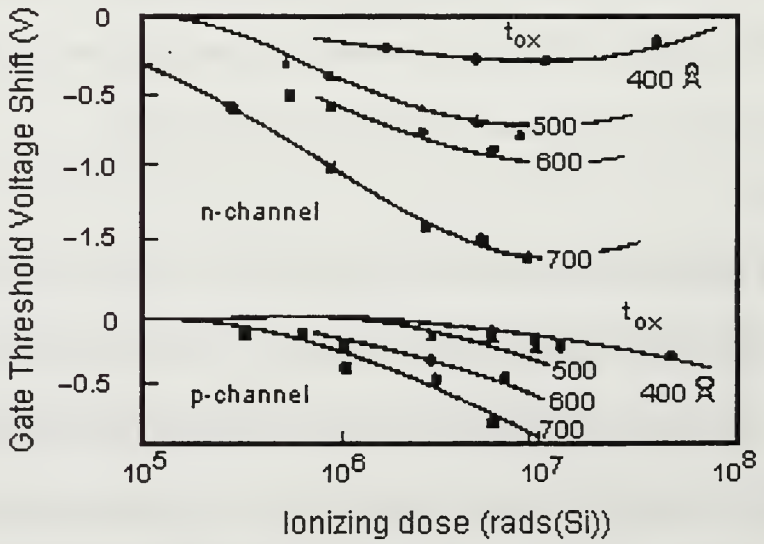


Figure 2.3. Threshold voltage shifts vs. radiation for varying gate oxide thicknesses from Ref. [7].

b. Leakage Current

Increase in leakage current is another effect of charge trapping and ionizing radiation. Typical leakage currents for commercial devices are on the order of 10 pA/cm^2 per rad (Si)/sec. The field oxide can be sensitive to ionizing radiation, which can cause an increase in leakage currents. This is a common cause of failure in MOS devices. Typical devices have been known to fail at doses of less that 10 krad (Si). [Ref. 7]

Just as holes are trapped at the Si-oxide interface, so are they trapped along the field oxide-silicon substrate boundary, as shown in Figure 2.4 [Ref. 4]. This area is called the "Bird's beak" region because of the way the field oxide narrows as it gets closer to the gate oxide. Trapped positive charge in this region attracts electrons and creates an end-around leakage current regardless of gate voltage. A parasitic transistor is created, passing current around the edge of the intrinsic device regardless of what state the transistor gate is in. This does not usually come into play for commercial applications and so is not monitored by most fabricators. [Ref. 4]

4. Dose Rate Effects

Just as the accumulation of charge over time causes extraneous currents to flow in a device, so can large transient bursts of ionizing radiation. With large enough transients, these currents can be comparable to and even greater than the currents caused by the normal operation of the device.

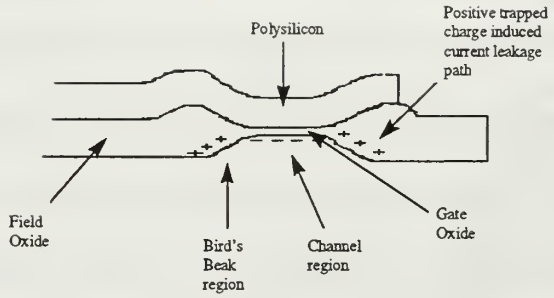


Figure 2.4. Cross sectional view of the bird's beak region of a MOS transistor after Ref. [4].

a. Upset

Transient currents, if present in the right areas and at the right magnitudes, could result in a change of state of a digital circuit. This is known as an upset. As long as the device does not burn out due to excessive current, the device can be returned to proper operation. The upset threshold is the lowest radiation dose rate that causes an upset, for dose-rate induced upsets. For single event upsets, the upset threshold is the lowest energy density per unit length due to an ionization track that can cause an upset.

b. Latch-up

As with total dose ionization, a device could receive enough of a transient burst of radiation from a non-ionized dose or an individual particle, to put it in a state where the parasitic circuits are turned on. This is called latch-up and will be explained further in the section on single event effects. In some devices, latch-up is known to exist over a limited set of dose rate levels called latch-up windows. A succession of these

windows is known to occur for lower dose rates of around 10^8 rads (Si)/sec. Upsets are generally thought of as pertaining to flip flop and memory circuits whereas latch-up normally refers to a particular device within a circuit. [Ref. 7]

c. Rail Span Collapse

The predominant dose rate effect is rail span collapse [Ref. 23]. Rail span collapse is the temporary reduction in V_{dd} and increase in V_{ss} due to the rise in photo-current caused by the incident radiation pulse. This current flows from the device into the V_{dd} and V_{ss} metallization runs. Because of the finite resistance offered by the metallization, neighboring devices see the V_{dd} and V_{ss} changes and their function becomes impaired. [Ref. 7] If the radiation-induced transient current is great enough, it can cause electromigration of the power and ground rails [Ref. 24].

B. SINGLE EVENT EFFECTS (SEEs)

Single event effects are similar to those previously described but they are caused by the passage of a single energetic particle through a critical area of the device, which is referred to as the sensitive cross section. As the single particle penetrates the device, it deposits energy along its path either directly or through nuclear reactions with the device material. This can change the state of a flip flop or a logic gate, which can change the information stored in the system, cause erroneous commands to be issued, undefined

states to be attained, etc. Also, single events can cause latch-up with the possibility of device burnout or destruction of the gate. [Ref. 2]

1. Single Event Upset

Single event upset is the changing of information due to a single particle strike. Information is represented in a CMOS circuit or storage device by voltage levels. Usually, logic 0 = 0V and logic 1 = +5V or +3.3V for low-voltage CMOS. For example, in a DRAM circuit, information is stored on capacitors. A certain amount of charge must be present on the capacitor to cause a certain voltage to appear across the capacitor and represent the correct logic value. If an incident particle is energetic enough, the charge produced could either charge or discharge the storage capacitor, thereby changing the stored information. This is termed a soft error. Provided the induced current is not large enough to cause device burnout, the device can still function properly although the data will need to be corrected. Usually, data encoding and other circuit design features are used to correct for such errors and prevent the upset of one device from affecting the operation of the entire system.

2. Single Event Latch-up

SEL is a more serious problem because it can result in destruction of the device. Latch-up is associated with the parasitic p-n-p-n semiconductor structures that are an inherent part of the CMOS fabrication process [Ref. 4]. Figure 2.5 shows these parasitic elements. The BJT inside the n-well is called the vertical transistor because it is formed by

the vertical p-n-p of the doped region, n-well and p-substrate. The other transistor in the figure is called the lateral BJT for similar reasons. Once these parasitic devices are triggered, a self sustaining avalanche effect takes over, producing very high currents [Ref. 8]. Removing and resetting power will remove this condition, again, assuming burnout has not occurred. [Ref. 7]

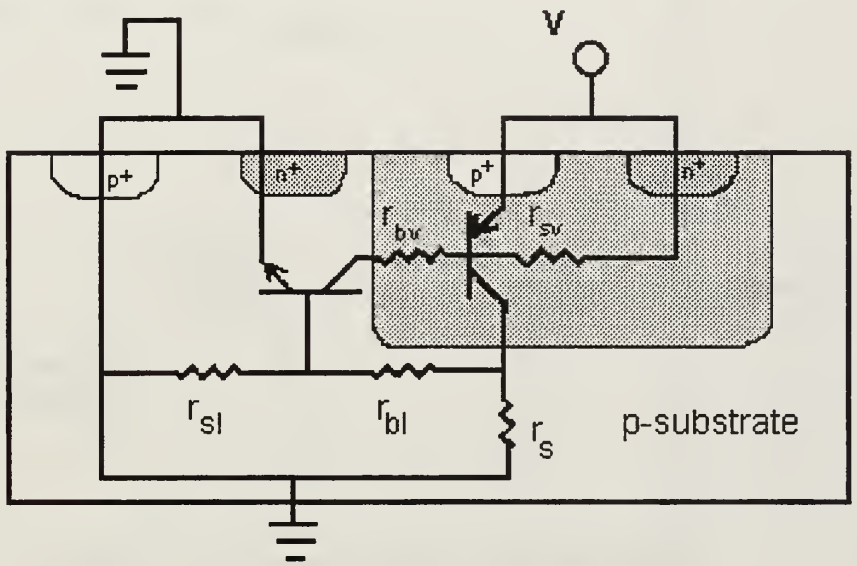


Figure 2.5. Parasitic BJT elements for a standard CMOS device after Ref. [8].

In SEL, these elements are turned on by the transient currents and voltages produced by the ion strike. Latch-up can also occur as a result of improper substrate or well biases or due to elevated temperatures. The increased temperature acts to reduce V_{be} of the parasitic BJTs making them easier to turn on. Once on, the positive feedback of the parasitic circuit leads to latch-up. [Ref. 8] This is a common mode of failure for commercial microcircuits in radiation environments [Ref. 4].

The I-V characteristics for the parasitic circuit are shown in Figure 2.6. There are three regions to this curve as shown: the on region, the forward blocking region and the breakover region.

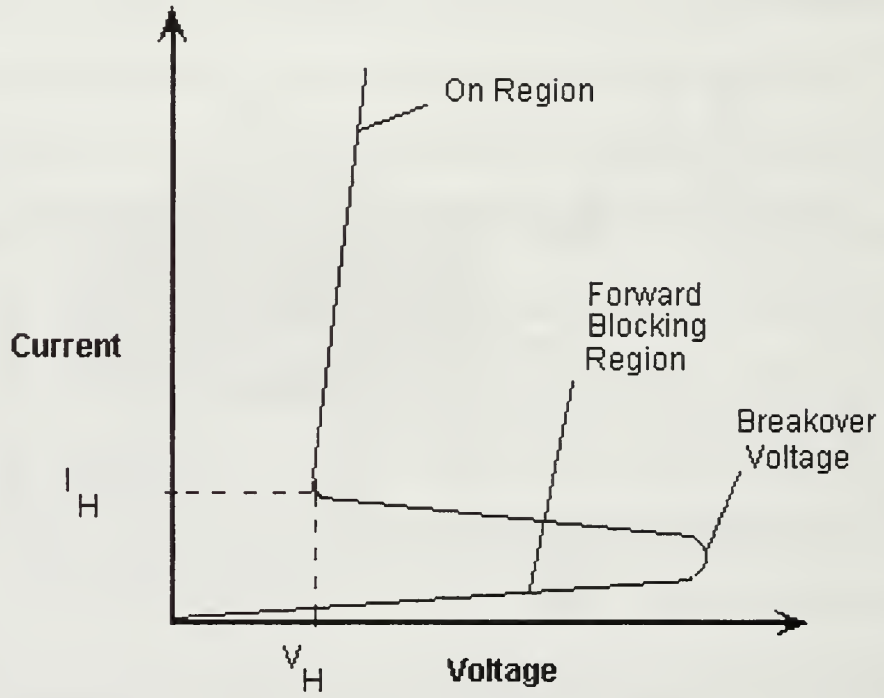


Figure 2.6. I-V characteristics for a latch-up vulnerable p-n-p-n structure after Ref. [8].

Catastrophic failure can occur without exceeding the breakover voltage. Any event placing the device into the on region can trigger latch-up. If the vertical BJT turns on first, it is referred to as anode triggering. This is the more common event. Cathode triggering is when the lateral transistor turns on first. As long as the holding voltage, V_H, is not exceeded, the device cannot enter the on region. The holding voltage is the lowest

voltage necessary for the device to be in the on region. Designing the circuit so that V_H is greater than the supply voltage is the normal method used to try to prevent SEL.

All of these effects must be taken into account for any system which will be used in a space environment. The next chapter presents the test designs which were fabricated to combat some of these effects.

III. EXPERIMENTAL TRANSISTORS

The two chips that were tested for this research were specifically designed for radiation effects research at the Navy Postgraduate School. Both chips were manufactured by Orbit Semiconductor through the MOSIS Service of the Information Sciences Institute at the University of Southern California in Marina del Rey. The MOSIS lot average parametric test results are presented in Appendix A.

The purpose of these chips is to evaluate a new experimental method for compensating for the threshold voltage shift and reducing or eliminating gate end-around leakage. Each chip contains three different designs called structures. For each structure there are six different transistors, three pFETs and three nFETs. Each of the three pairs is a different size. Diagrams of these devices are presented in Appendix B. A description of these transistors follows.

A. CHIP ONE PART #N69P AP

1. Structure #1

This structure uses traditional transistor designs with an added feature. A second polysilicon gate or bias control gate is provided over the bird's beak region. This bias gate is the same length as the control gate. All transistors on both chips have guard rings around them to provide isolation from adjacent devices. NFET #1 and pFET #1 are the

same size, as are the #2 nFET/pFET pair and the #3 nFET/pFET pair. This is true of all structures on both chips. Transistor one has a channel that is two microns long by eight microns wide. Transistor two has a channel that is two microns long by twenty four microns wide. Transistor three has a channel that is two long and forty four microns wide.

2. Structure #2

The second structure on chip one has a bias gate that extends across the entire channel. It is the same length as the polysilicon control gate and is directly over it, assuming no misalignment in fabrication. These three sets of transistors are sized 2x4, 2x20 and 2x40 (length x width) for set one, two and three respectively.

3. Structure #3

Structure three is used as the control group. There is no bias gate for these devices. Their sizes are the same as for structure two: 2x4, 2x20, and 2x40.

B. CHIP TWO PART # N69P BP

1. Structure #1

Structure one contains a bias gate region over the bird's beak region only. The difference from chip one is that this bias region is four microns wider than the gate, extending two microns on either side. Channel sizes are 2x8, 2x24, and 2x44 (length x width).

In the second structure, the gate bias region extends over the entire channel and is four microns wider that the gate. Channel sizes are 2x4, 2x20, and 2x40 (length x width).

3. Structure #3

Structure three is the control group with no additional gate bias region and channel sizes of 2x4, 2x20, and 2x40 (length x width).

The intention for these designs is that the second bias gate over the bird's beak region would be effective in stopping or reducing the end-around gate leakage. By extending the gate bias region over the entire channel, it was anticipated that this would counter the shift in threshold voltage due to radiation exposure. The tests that were conducted to determine whether or not these designs were successful will now be discussed.

IV. TESTING

The main objective of the testing was a proof of concept. The focus was on showing that the new designs are more radiation tolerant than the control transistors and that the threshold voltage and/or subthreshold leakage current can be influenced by applying a voltage to the gate two bias.

Due to laboratory facility availability constraints, only the devices from chip one were tested. The transistors on the first chip were determined to be more promising. Only the two larger transistors of each structure were tested in order to obtain the maximum amount of data for each structure within timing limitations.

Throughout this work, transistors are identified by the following nomenclature: chip number, transistor type, transistor size and structure, in that order. For example, transistor 1N23 is an N-type transistor on chip one. It is the middle size device (one being the smallest and three being the largest), and it is from structure three as described in the previous chapter.

A. INITIAL TESTING

All devices were first placed on a curve tracer to ensure that they exhibited normal CMOS I-V characteristic curves which all devices on chip one did. Structure two devices

for chip two did not function properly. This was another factor in the decision not to test chip two.

Each nFET was then tested using a Hewlett-Packard 4145B parameter analyzer with a compliance of 1mA. The control gate voltage, V_g, was varied from -1V to 4V with the gate two bias, V_{g2}, set to zero and V_{ds} set at a constant 0.1V. A plot of I_d vs. V_g was taken for each device. The maximum transconductance was also recorded and plotted along with the I-V curves and is displayed as the variable mu along the left hand axes of the plots in Appendix C. The same was done for the pFETs with V_g varied from 1V to -4V and V_{ds} = -0.1V. The order of device testing was n-type first, smaller to larger, structure one to three. This order was maintained throughout.

Also for each device, I_d was measured for $V_g = V_{g2} = 0V$ and $V_{ds} = 5V$ to measure the leakage current through the transistor in a state where it would be off for original threshold voltage conditions. If the device remained unaffected by the radiation, 0V would be less than the required threshold voltage and V_{ds} would be a maximum.

B. RADIATION DOSES

Next, the chip was subjected to 10 krad(Si) using a Gammacell 220 Co-60 source at Lockheed-Martin Missiles & Space in Sunnyvale, CA. The source delivered a dose rate of 17.666 rad(Si)/sec. During irradiation, the gate two bias was shorted to all source

and drain connections while the control gate was biased at a positive five volts. The chip was irradiated five times and measurements taken for total doses of 10, 20, 40, 80 and 160 krad(Si).

C. DATA COLLECTED

Upon completion of irradiation, the above mentioned HP 4145B information was again obtained. The gate two bias was then adjusted to determine if it would effect the threshold voltage or subthreshold leakage current. For the threshold voltage measurements, V_{ds} was set to +/- 0.1V (+ for n-type and - for p-type devices) and the control gate voltage was swept from -1V to 4V and 1V to -4V for n and p-type transistors respectively. The control gate voltage was adjusted as necessary to view device transition. The threshold voltage was chosen to be the point at which $I_d = 1\mu A$, in accordance with industry practice.

For the leakage current measurements, V_{ds} = +/- 5V and the control gate voltage was swept from 1V to -1V with the value at $V_g = 0$ recorded.

Measurements for 80 and 160 krad were taken two weeks after the measurements for Pre-rad, 10, 20, and 40 krad due to facility availability. Measurements were taken prior to starting the second day of irradiations on order to detect any annealing effects in

the devices. The chip was kept at room temperature and all connections were short circuited during the two week period.

V. RESULTS

The results of the radiation testing described in Chapter IV are tabulated and plotted in Appendix C. These tables show the maximum transconductance observed within the transition window plotted. Also displayed is the threshold voltage at 1 μA and the subthreshold leakage current at V_{ds} = 5V. All data is with V_{g2} = 0V. A brief summary follows.

A. STRUCTURE ONE

1. NFETs

a. Subthreshold Leakage Current

As expected, the subthreshold leakage current increased with each increase in radiation dose, as seen in Tables C.1 and C.2. The slope of the I-V curve transition area (Figures C.21 - 27) also decreased. This is caused by the trapped positive charge in the gate and field oxides attracting majority carrier electrons [Ref. 4]. From Tables C.1 and C.2, it can be seen that at lower radiation doses, the larger transistor (2x40 LxW) had a smaller leakage current than the smaller 2x20 transistor. However, in Figure C.48, for higher doses, the larger transistor was determined to have been on continuously with the leakage current greater than 1 μA at all values of control gate voltage. For both size transistors, I_d vs. radiation dose graphs exhibit the same shapes. With the exception of Figure C.32, a decrease in the gate two bias (V_{g2}) voltage was able to lower the

subthreshold leakage current as evidenced by Figures C.33 - 35 and C.53 - 56. However, the pre-radiation current levels of Tables C.1 and C.2 could not be achieved.

b. Threshold Voltage

With regard to threshold voltage and Figure C.7, the smaller of the two transistors was more erratic, first shifting positive and then shifting more negative than the larger transistor. Although a subthreshold leakage current greater than one microamp would not allow a consistent threshold voltage determination in Table C.2 at 160 krad(Si), the transition midpoint of 1N31 from Figure C.48 is at approximately 0.4V, as opposed to the negative threshold voltage of device 1N21 from Figure C.27 and Table C.1. This would imply that the larger device experienced less threshold voltage shift than did the smaller device.

Figures C.58 and C.59 show that adjusting the gate two bias voltage appeared to have no effect on the threshold voltage of the larger 2x40 (LxW) device. This device only has gate two coverage over the bird's beak region and it would appear that it is too far removed from the channel to shift V_t. Refering to Figures C.38 - 40, however, it is clear that the smaller device experienced a large effect. An increase in magnitude of V_{g2} correspondingly increased the threshold voltage. Positive voltages were not applied to the gate two bias in an attempt to shift V_t more negative at the earlier radiation doses where the threshold voltage had increased because this design was targeted more toward adjusting the end-around gate leakage. Positive V_{g2} voltages were

applied to 1N21 at 80 krad and were successful at lowering the threshold voltage. Pre-radiation threshold voltage values from Tables C.1 and 2 were obtained by adjusting V_{g2} for all cases where attempted. For all radiation levels, a more negative V_{g2} raised V_t (Figures C.37 - 40).

2. PFETs

b. Subthreshold Leakage Current

The subthreshold leakage currents for all pFETs (Tables C.7 - 12) were not significant at the radiation doses they were exposed to. Structure one devices experienced only an 18% current increase and no p-type device had a leakage current of more than 16 pA for all three structures. The leakage current of most devices was on the order of tens of picoamps. Current shifts due to gate two bias voltages were insignificant at less than 1 pA.

b. Threshold Voltage

As evidenced in Figure C.10, both the larger and smaller transistors experienced similar threshold voltage shifts as a function of total dose received. Similarly, both devices shifted in the negative direction. The gate two bias had no effect on either device until the 160 krad dose was reached (Figure C.142). At this total dose level, the larger device experienced an increase in V_t with a corresponding decrease in V_{g2}. The original pre-radiation threshold voltage from Table C.8 was again achieved.

The smaller transistor was not operational at this radiation level. It is believed that this was caused by ESD damage during the experiment. No ESD protection circuitry was included on either test IC design to prevent radiation-induced changes in ESD protection circuits from influencing the sensitive measurements of the FET parameters. Figure C.143 is provided as a linear assumption of V_{g2} - V_{to} correlation vs. radiation dose but data was not obtained to confirm this. The change in threshold voltage as a function of gate two bias is seen to be linear at 160 krad (Figure C.142).

B. STRUCTURE TWO

1. NFETs

a. Subthreshold Leakage Current

As with structure one, the subthreshold leakage current for both size transistors increased with radiation dose (see Tables C3 and 4). In this case, the smaller device experienced greater degradation than the larger device as seen in Figure C.2.

V_{g2} had no conclusive effect on the subthreshold leakage current of the smaller device (Figures C.71 - 75). This 2x20 transistor became permanently on at 160 krad (Figure C.66)as defined by the amount of leakage current which was never below 3 μA. The 10 and 20 krad dose curves (Figures C.71, 73, 92 and 93) have the same shape for both size devices. In Figures C.74 and 75 for 1N22 at 40 and 80 krad, a decrease in I_d

was observed but due to limited corroborating data, no consistent effect can be determined.

b. Threshold Voltage

The smaller device showed no effects from a change in gate two bias (Figures C.77 - 80). Voltages down to -16V were applied with less than 0.1V change in V_t. The 2x40 (LxW) device responded well to V_{g2} shifts in Figures C.95 - 98. A decrease in V_{g2} raised the threshold voltage almost linearly at all radiation levels. The pre-radiation value from Table C.4 was easily obtained each time. Figure C.99 shows the value of V_{g2} necessary to return the device to a value of 0.7592V, the pre-radiation value. This plot is roughly linear as well.

2. PFETs

a. Subthreshold Leakage Current

As mentioned above, there was no significant change in subthreshold leakage current at the tested radiation levels. Tables C.9 and 10 show very similar values for all radiation levels.

b. Threshold Voltage

As with the nFETs, the smaller device was unaffected by changes in the gate two bias as seen in Figures C.154 - 156. This device, 1P22, also experienced a catastrophic failure at 160 krad(Si), the same as transistor 1P21. The failure is believed

to have been a non-radiation problem and probably caused by ESD. The larger device was unaffected by V_{g2} at doses below 40 krad (Figures C.168 - 170). Above 40 krad (Figures C.171 and 172), V_{g2} was able to restore V_t to its pre-radiation value in Table C.10. At 160 krad though, this was accompanied by a significant increase in the slope of the transition portion of the I-V curve as seen in Figure C.164.

VI. CONCLUSION AND RECOMMENDATIONS FOR FURTHER STUDY

A. DEVICE PARAMETER COMPENSATION

It is likely that some FET parameter values changed between the completion of irradiation and the testing of the individual device. However, during post irradiation device measurements, the same order was maintained for measuring each device. Furthermore, rather than testing specific device parameters, more emphasis was placed on the comparison between the test designs and the control transistors. By testing the control devices last, they were afforded more time to rebound (anneal), making for worst case testing. The studied designs may have been a greater improvement over the control models than demonstrated.

1. Structure One

Structure one was conceived primarily as an attempt to decrease the end-around gate leakage current. In this regard, the design is considered successful. Both sized nFET devices tested were able to reduce the subthreshold leakage current by decreasing the voltage on the second gate. Although the second gate voltage could not return the leakage current to pre-radiation values, it was reduced by 37% or greater (with the exception of transistor 1N21 at a dose level of 10 krad(Si) (see Figure C. 32).

The effect seemed to reach a practical limit, however. Second poly voltages greater in magnitude than 16V were not tried because charge tunneling through the thin oxide between the two poly layers could initiate at voltages above 16V. The leakage currents present in the pFETs were not large enough to glean any realistic data from. As pFETs are inherently more radiation tolerant due to the electron-hole mobility difference mentioned in Chapter II, it is recommended that higher radiation doses be examined. It is apparent that these devices have not yet reached a state in which the effectiveness of the design can be determined.

The smaller n-type device experienced less of a shift in threshold voltage than did the larger device. It is possible that the second polysilicon material was too far away to have any affect on the channel charge carriers. The 2x20 (LxW) p-type transistor was destroyed before the higher dose tests but the 2x40 device was able to alter the threshold voltage at 160 krad(Si). This implies that the second poly gate may not be having a direct impact on the channel or the end-around leakage but may be responsible for shifting some of the interfering accumulated charge out of the way. More study at higher total dose levels is required to determine if this is only a temporary charge movement. This is not the way in which the design was conceived to operate, although it may still accomplish the same goals.

2. Structure Two

The larger devices, both n-type and p-type, were successful in raising the poly-one gate threshold voltages. Once again, the pFET only at higher radiation doses. The n device exhibited linear behavior. However, neither of the smaller devices had any effect. This inconsistency makes it difficult to determine if the design is successful, if the device size is the deciding factor, or if some additional unknown effect is responsible. The response of the larger devices would indicate that this concept may still prove fruitful.

B. RADIATION TOLERANCE

With regard to improved radiation tolerance, both designs were successful. In nearly all cases, the devices of structures one and two retained higher threshold voltages and lower leakage currents. In particular, three of the four V_t structure comparisons (Figures C.17, C.19, and C.20) remained fairly stable while the control devices had a large ΔV_t. The second poly gate was able to absorb some of the radiation, allowing the transistor to be less effected.

The benefit of these designs is that they afford some improvement in tolerance while still using a bulk CMOS process. These devices can be fabricated with only minor mask changes.

C. RECOMMENDATIONS FOR FURTHER STUDY

Due to the small radiation effects on most of the p-type devices, more study of these designs at higher radiation doses in needed. Much of the evidence is inconclusive for the levels studied here. The leakage currents had not yet made any appreciable change and the gate two bias was just beginning to have an influence on a number of devices. Post irradiation annealing should also be looked at.

It is also recommended that all HP 4145 data be recorded on disk for easier access and recall. Some of the higher dose rates were returned to pre-radiation threshold voltage values but with a change in I-V transition slope. The change in transconductance could be more accurately quantified.

Further test structures should attempt to include the use of channel stops as another means of reducing the end-around leakage current. The value of channel stops may not be realized in a p-type device due to the low currents observed here. Additional components should employ the devices in inverters and/or ring oscillators for power, noise margin and timing comparisons.

It is strongly recommended that a separate pin be provided for the second gate bias for each transistor or group of transistors within the same implementation. By

one V_{g2} pin for the nFETs and one for the pFETs, devices not yet being looked at were having their gate two bias voltage adjusted. It is likely that this had an effect on the state of border and interface traps as well as trapped charge within the material.

The possibilities in this area are very exciting and this thesis shows that not only could radiation hardened devices be fabricated from standard non-hardened processes and therefore at cheaper prices, but the compensation from the second poly gate could allow for a relatively simple feedback circuit to compensate the on board devices, greatly extending the active service life of our space systems. Testing with higher radiation levels and follow-on annealing tests should confirm the initial indications of this study of the effectiveness of these design techniques as well as gate two bias required to compensate for the radiation effects.

APPENDIX A. MOSIS FABRICATION LOT AVERAGE PARAMETRIC TEST RESULTS

DESIGN PACKING SLIP

SHIPPED BY:

The MOSIS Service
Information Sciences Institute
University of Southern California
4676 Admiralty Way
Marina del Rey, CA 90292-6695
Phone: 310/822-1511
Fax: 310/823-5624

DESIGN SUBMITTED BY:

Dr. Douglas J. Fouts
Associate Professor
Dept. of Elect. & Comp. Eng.
Code EC/FS
Naval Postgraduate School
Monterey, CA 93943
Phone: 408-656-2852

Date Shipped	Mosis Account	Customer PO	PO Release
30-DEC-96	309-NSF-CLASS/NPS-EC		

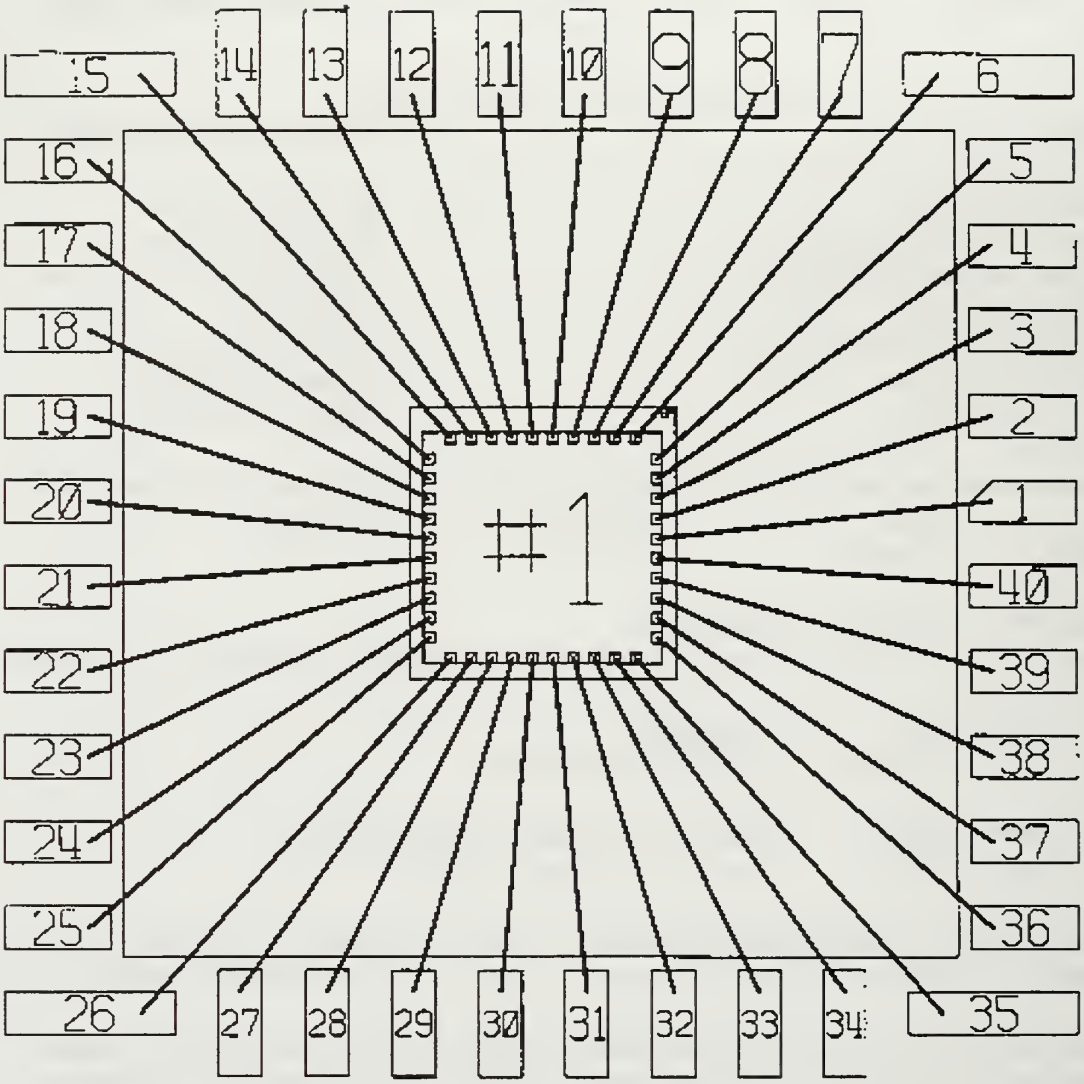
Quan	Unit	Part #	Description
		N69PBP	49564 RADTESTTWO
1	LOT	10194	Initial lot of 4 CMOS 2 µm, Tiny-Chip.
4	EACH	2011	Packaging: packaged in DIP40

Enclosed is a copy of the bonding diagram used to assemble your parts. If one of the pins was conneted to the substrate, that pin will be marked with an asterisk on the bonding diagram.

We are very interested in receiving your feedback about the quality of this fabrication and the performance of your parts. You can send a report to MOSIS via email using the instructions in Chapter 4 of the MOSIS User Manual, or you can send the enclosed report form to:

Customer Reports
The MOSIS Service
USC Information Sciences Institute
4676 Admiralty Way
Marina del Rey, CA 90292-6695

Enclosures: N69P.PRM file (parametric test data and SPICE parameters)
Bonding diagram for N69P-BP
MOSIS custromer report form



N69PBP

309-NSF-CLASS/NPS

#1: 49564/FOUTS/RADTESTTWO TINY CHIP

CIP40: 4 PARTS

11-SEP-1996

MOSIS PARAMETRIC TEST RESULTS

RUN: N69P VENDOR: ORBIT
TECHNOLOGY: SCNA20 FEATURE SIZE: 2.0 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parametrs obtained from similar measurements on a selected wafer are also attached.

COMMENTS: Orbit Semiconductor 2.0 µm n-well.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3/2			
Vth		0.87	-0.95	Volts
SHORT	18/2			
Vth		0.78	-0.92	Volts
Vpt		12.9	-15.1	Volts
Vbkd		12.7	-15.3	Volts
Idss		144	-70	µA/µm
WIDE	120/2			
Ids0		-11.4	2.2	pA
LARGE	50/50			
Vth		0.81	-0.91	Volts
Vjbkd		16.0	-17.0	Volts
Ijlk		13.0	-0.8	pA
Gamma		0.21	0.65	V^0.5
Delta length (L_eff = L_drawn-DL)		0.38	0.29	microns
Delta width (W_eff = W_drawn-DW)		0.00	-0.92	microns
K' (Uo*Cox/2)		26.3	-9.4	µA/V^2

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	6/4			
Vth		0.82	-1.27	Volts
SHORT	12/4			
Vth		0.79	-1.25	Volts
LARGE	36/36			
Vth		0.78	-1.26	Volts
K' (Uo*Cox/2)		22.3	-7.5	µA/V^2

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>25.2	-13.3	Volts

BIPOLAR PARAMETERS	W/L	NPN	UNITS
2x1	2x1		
Beta		108	
V_early		68.8	Volts
Vce,sat		0.4	Volts
2x2	2x2		
Beta		106	
V_early		67.5	Volts
Vce,sat		0.3	Volts
2x4	2x4		
Beta		103	
V_early		65.8	Volts
Vce,sat		0.4	Volts
2x8	2x8		
Beta		100	
V_early		64.2	Volts
Vce,sat		0.9	Volts
BVceo		20.3	Volts
BVcvo		20.2	Volts
BVebo		7.9	Volts

PROCESS PARAMETERS	N+DIFF	P+DIFF	POLY	POLY2	METAL1	METAL2	N_WELL	UNITS
Sheet Resistance	26.1	57.0	22.2	20.9	0.05	0.03	2430	ohms/sq
Width Variation (measured - drawn)	0.44	0.11	-0.26	-0.25	-0.81	0.10		microns
Contact Resistance	16.3	24.1	9.9	11.6		0.04		ohms
Gate Oxide Thickness	396							angstroms

CAPACITANCE PARAMETERS	N+DIFF	P+DIFF	POLY	POLY2	METAL1	METAL2	UNITS
Area (substrate)	121	315	58		25	21	aF/µm^2
Area (poly)				480	39	23	aF/µm^2
Area (poly2)					39		aF/µm^2
Area (metal1)						45	aF/µm^2
Area (N+active)			871	702	43	26	aF/µm^2
Area (P+active)			865	697			aF/µm^2
Fringe (substrate)	537	387					aF/µm
Fringe (N+active)			60				aF/µm
Fringe (P+active)			58				aF/µm

CIRCUITS PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.12	Volts
Vinv	1.5	2.32	Volts
Vol (100 μA)	2.0	0.25	Volts
Voh (100 μA)	2.0	4.67	Volts
Vinv	2.0	2.46	Volts
Gain	2.0	-11.93	
Ring Oscillator			
MOSIS (31-stage, 5V)		38	MHz

N69P SPICE BSIM1 (Berkeley Level 4; HSPICE Level 13) PARAMETERS

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NM1  PM1  DU1  DU2  ML1  ML2
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*PROCESS=ORBIT
*RUN=n69p
*WAFER=03
*Gate-oxide thickness= 383 angstroms
*DATE=17 - Dec-1996
*
*NMOS  PARAMETERS
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 7.62079E-01, 0.00000E+00, 0.00000E+00
 1.39149E+00, -2.68387E-01, 5.02294E-02
 2.90550E-01, -7.17780E-03, -1.91881E-01
-8.98269E-03, 3.89355E-02, -1.55516E-03
5.61639E+02, 4.41901E-001, -4.12796E-001
5.37789E-02, 4.33455E-02, -8.15047E-02
3.19917E-02, 1.04488E+00, -5.90490E-01
6.51558E+00, -5.23038E+00, 7.79817E+01
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1.66001E-04, -2.52805E-03, -4.41578E-03
8.77125E-04, -4.43301E-05, 2.99906E-02
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-4.93320E+00, 2.25845E+01, 1.47556E+02
8.44588E+00, 7.24307E+01, -8.91594E+01
2.23344E-02, 4.55022E-02, -1.18707E-01
3.83000E-002, 2.70000E+01, 5.00000E+00
2.98815E-010, 2.98815E-010, 4.14416E-010
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1.00000E+000, 0.00000E+000, 0.00000E+000
0.00000E+000, 0.00000E+000, 0.00000E+000
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*Gate Oxide Thickness is 383 Angstroms
*
*PMOS  PARAMETERS

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2.01518E+02, 6.28638E-001, -3.91421E-001
1.18063E-01, 4.02274E-02, -1.23551E-01
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7.33185E+00, -5.57181E-01, 1.92791E+01
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-1.85363E-03, 1.90230E-03, -8.95086E-03
3.83000E-002, 2.70000E+01, 5.00000E+00
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0.00000E+000, 0.00000E+000, 0.00000E+000
*
*N+ diffusion::
*
26.1,    1.18e-04,      5.54e-10,      1e-08,   0.63
0.63,    0.697,         0.290,         0,       0
*
*P+ diffusion::
*
57,      3.22e-04,      3.98e-10,      1e-08,   0.90
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*
*METAL LAYER -- 1
*
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0,       0,       0,       0,       0
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*METAL LAYER -- 2
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0,       0,       0,       0,       0
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N69P SPICE LEVEL2 PARAMETERS

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+ UO=712,4 UEXP=1.1860E-01 UCRIT=8.3460E+03 RSH=2.4420E+01
+ GAMMA=0.6223 NSUB=9.4820E+15 NFS=9.0900E+10 VMAX=5.1820E+04
+ LAMBDA=3.7350E-02 CGDO=2.6007E-10 CGSO=2.6007E-10
+ CGBO=3.4582E-10 CJ=1.18E-04 MJ=0.697 CJSW=5.54E-10
+ MJSW=0.290 PB=0.63
* Weff = Wdrawn - Delta_W
* The suggested Delta _W is 2.0000E-09
.MODEL CMOSP PMOS LEVEL=2 PHI=0.700000 TOX=3.8300E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8667 DELTA=2.9480E+00 LD=1.4390E-07 KP=1.6490E-05
+ UO=182.9 UEXP=2.7910E-01 UCRIT=1.3010E+05 RSH=9.0910E-02
+ GAMMA=0.6632 NSUB=1.0770E+16 NFS=9.7480E+10 VMAX=9.9990E+05
+ LAMBDA=4.5020E-02 CGDO=1.9461E-10 CGSO=1.9461E-10
+ CGBO=4.9979E-10 CJ=3.22E-04 MJ=0.608 CJSW=3.98E-10
+ MJSW=0.223 PB=0.90
* Weff = Wdrawn - Delta_W
* The suggested Delta _W is -9.2280E-07
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APPENDIX B. CHIP DESIGN LAYOUTS

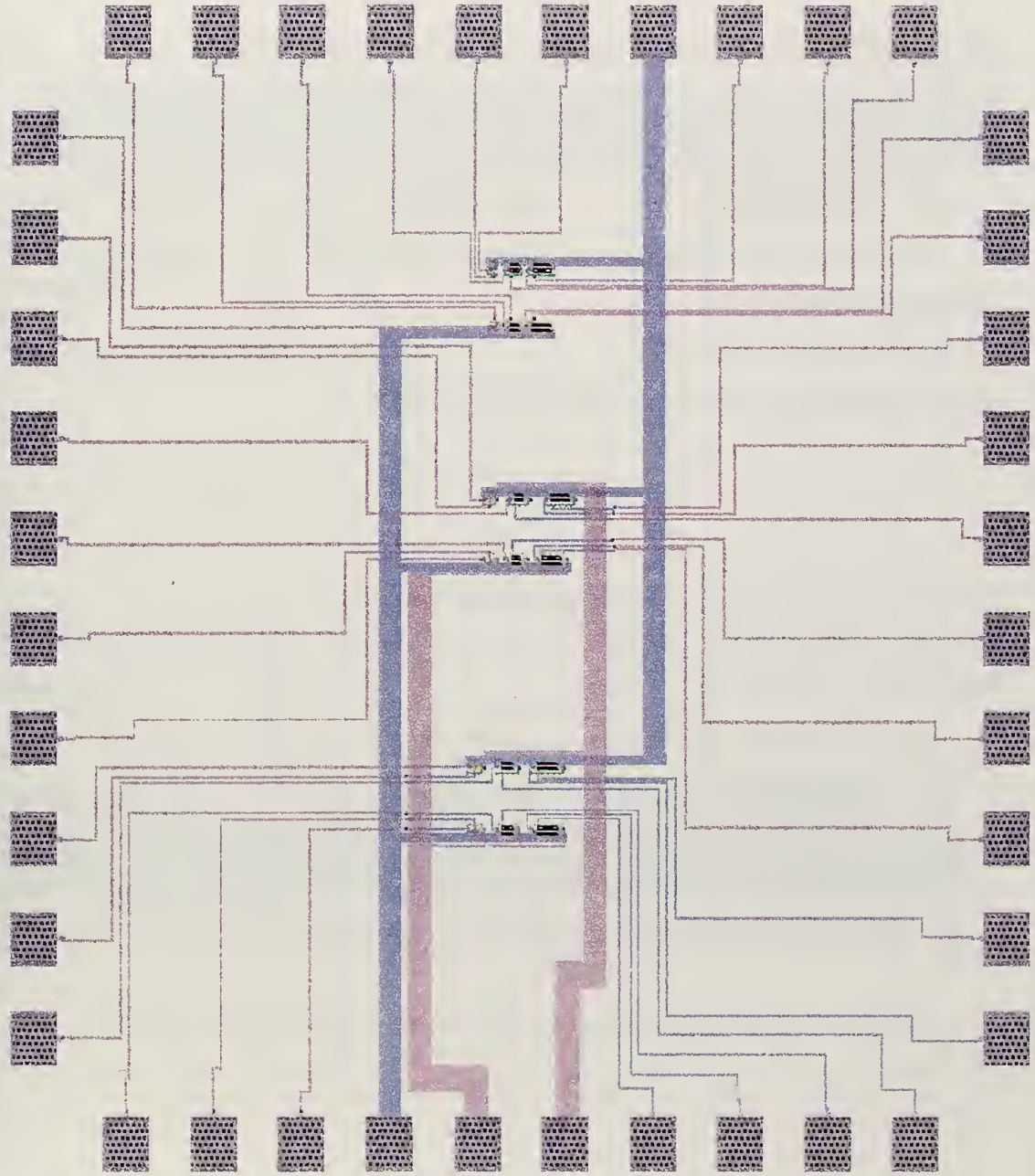


Figure B.1. Chip One layout.

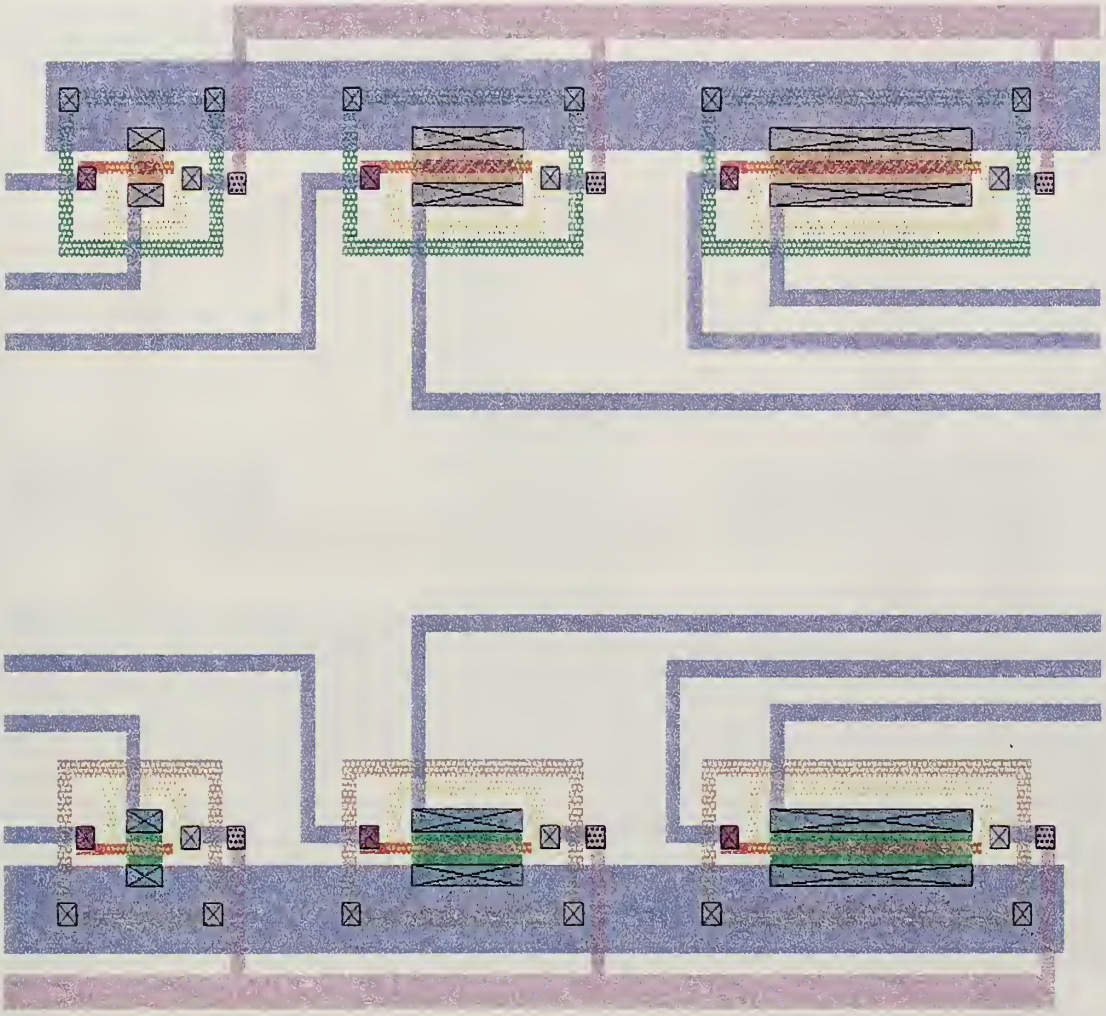


Figure B.2. Chip One Structure One (pFETs on top, nFETs on bottom).

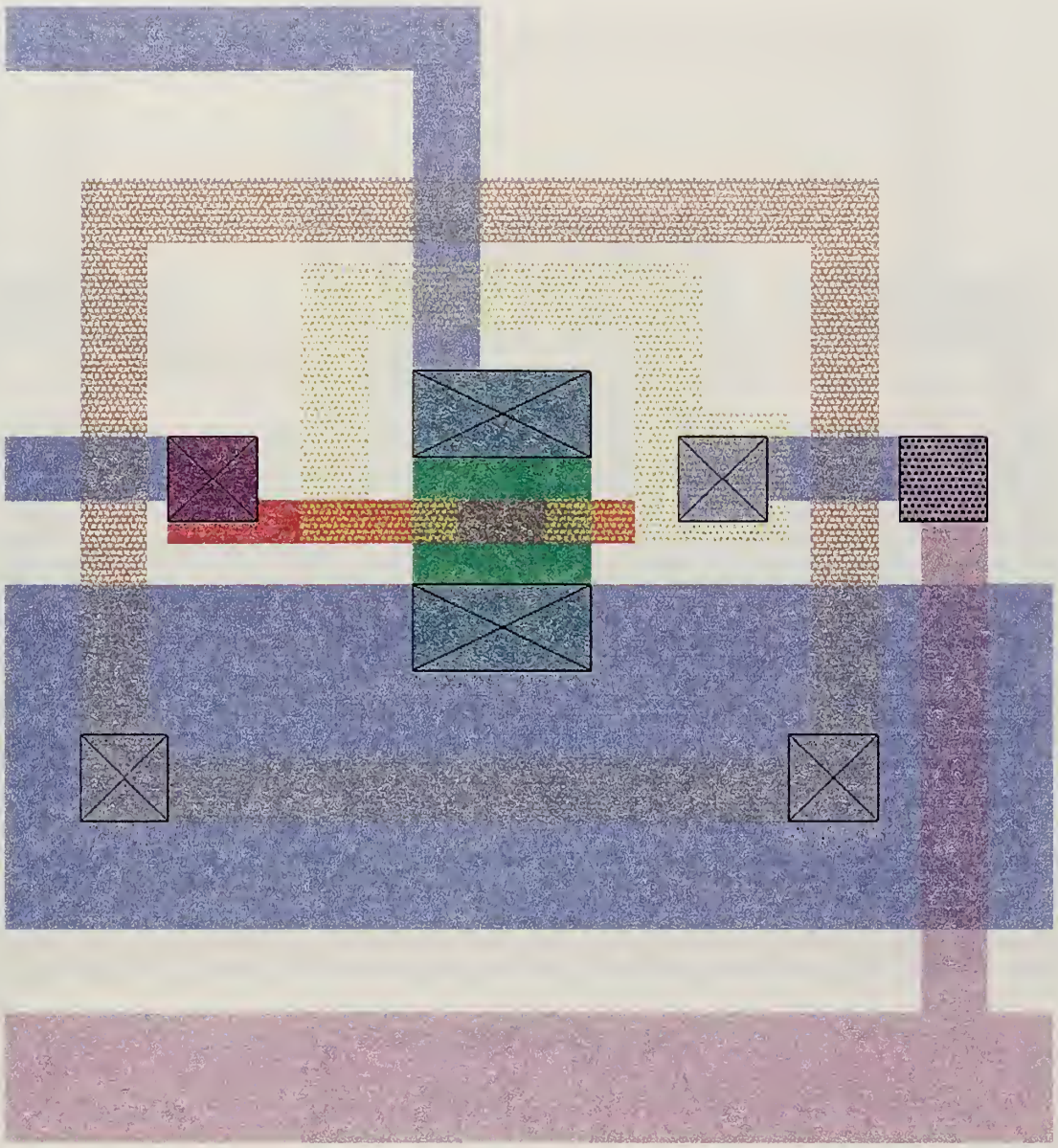


Figure B.3. Device 1N11.

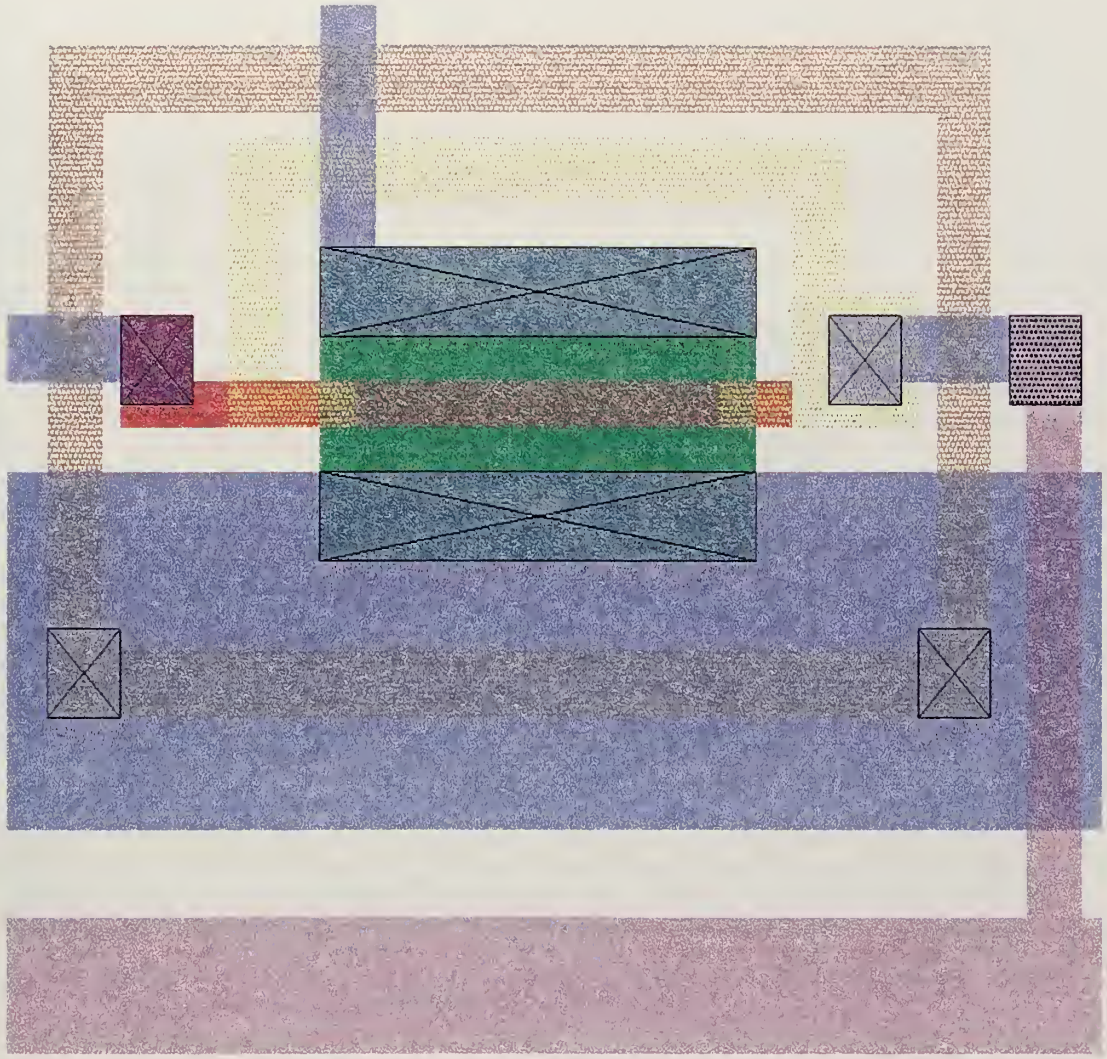


Figure B.4. Device 1N21.

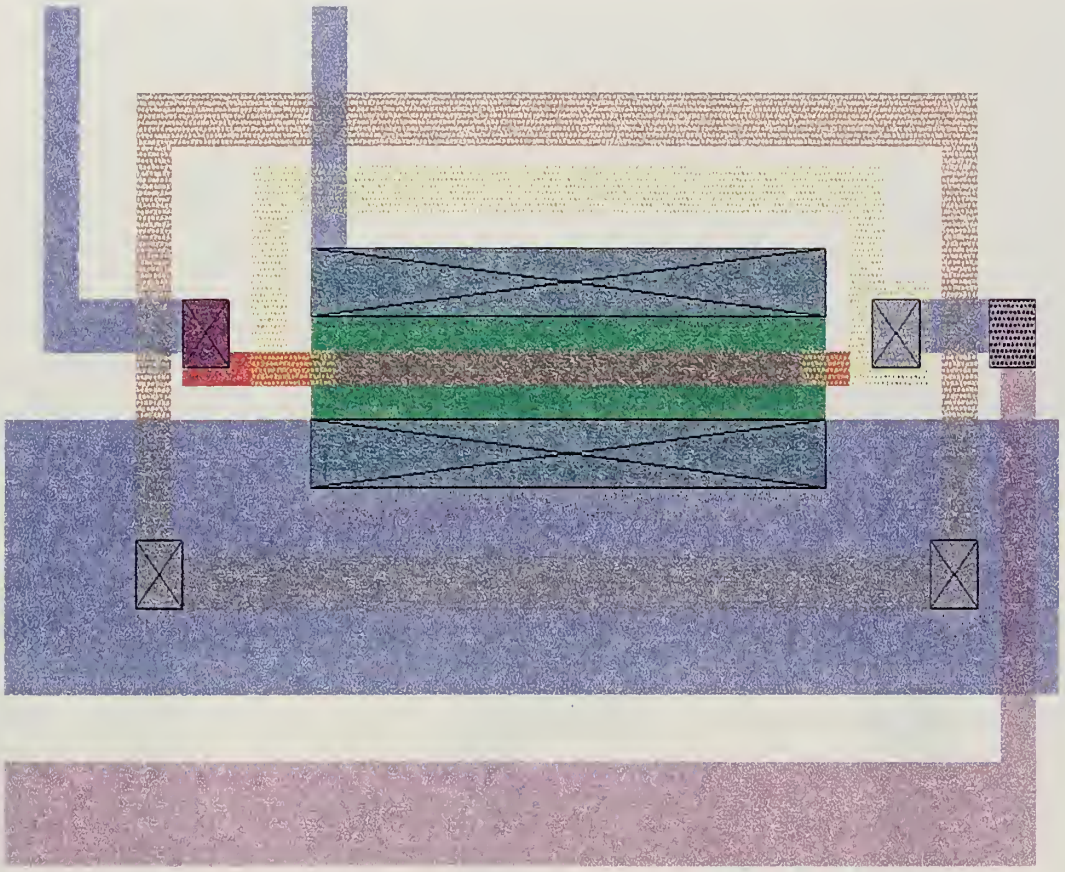


Figure B.5. Device 1N31.

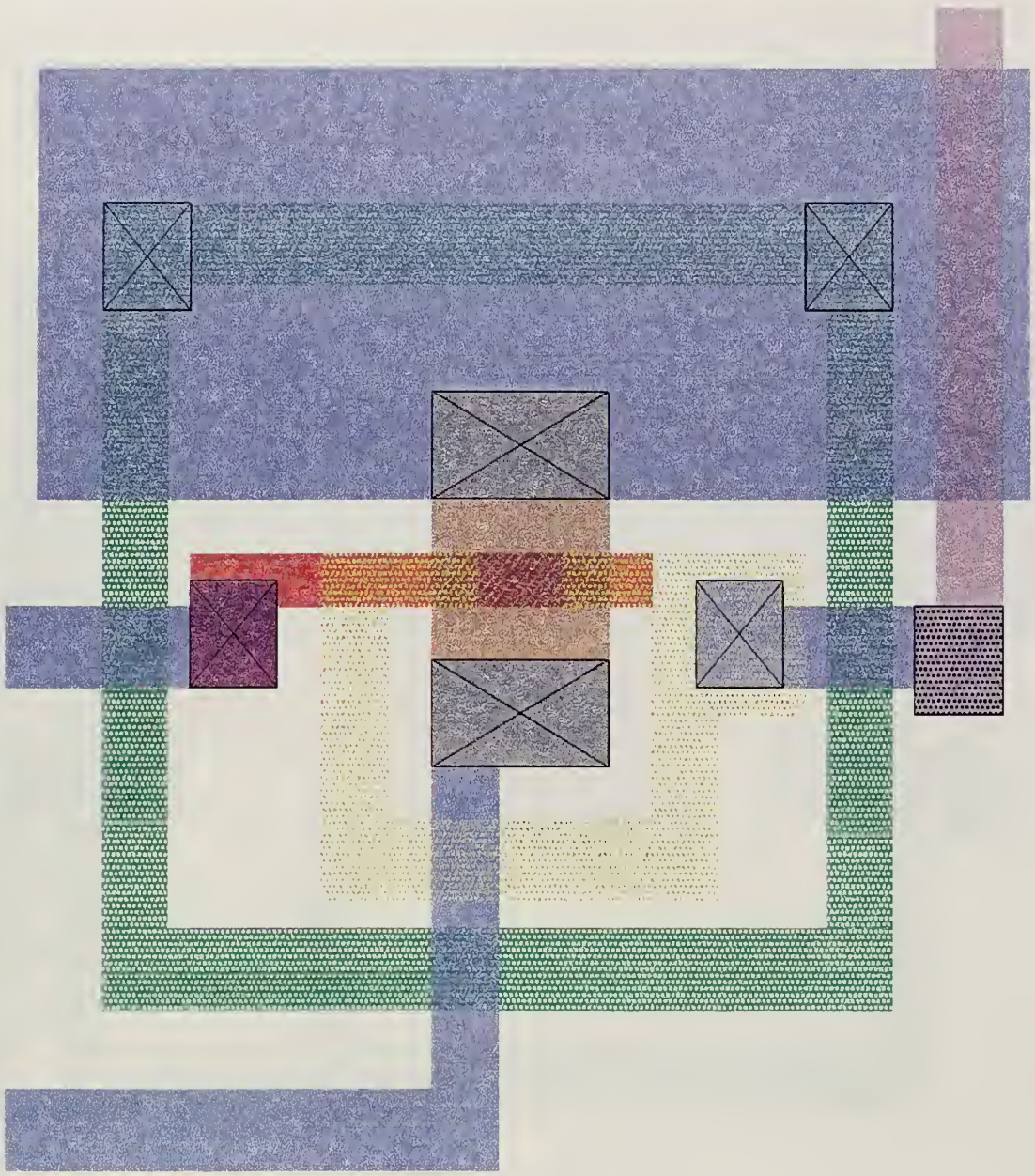


Figure B.6. Device 1P11.

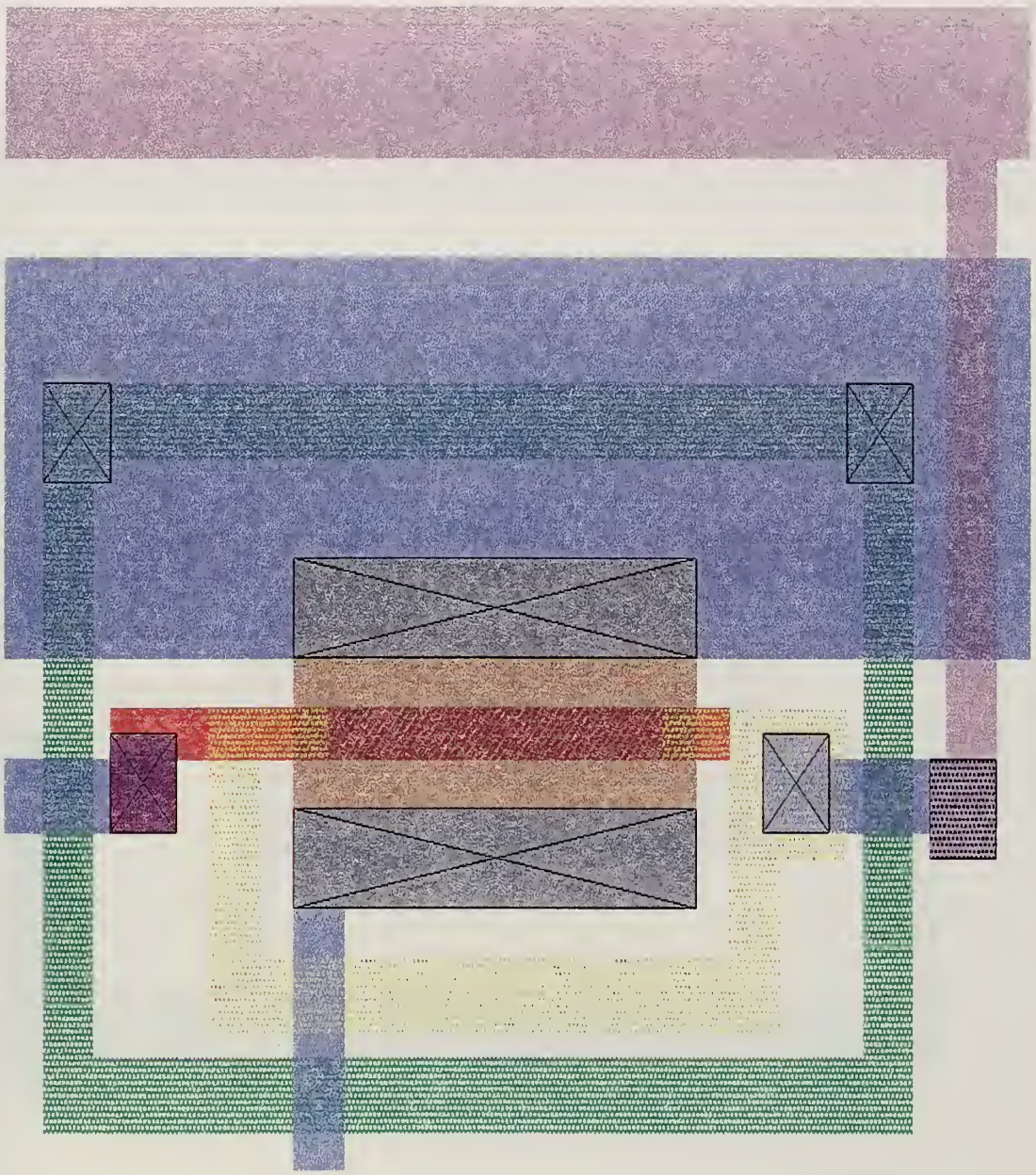


Figure B.7. Device 1P21.

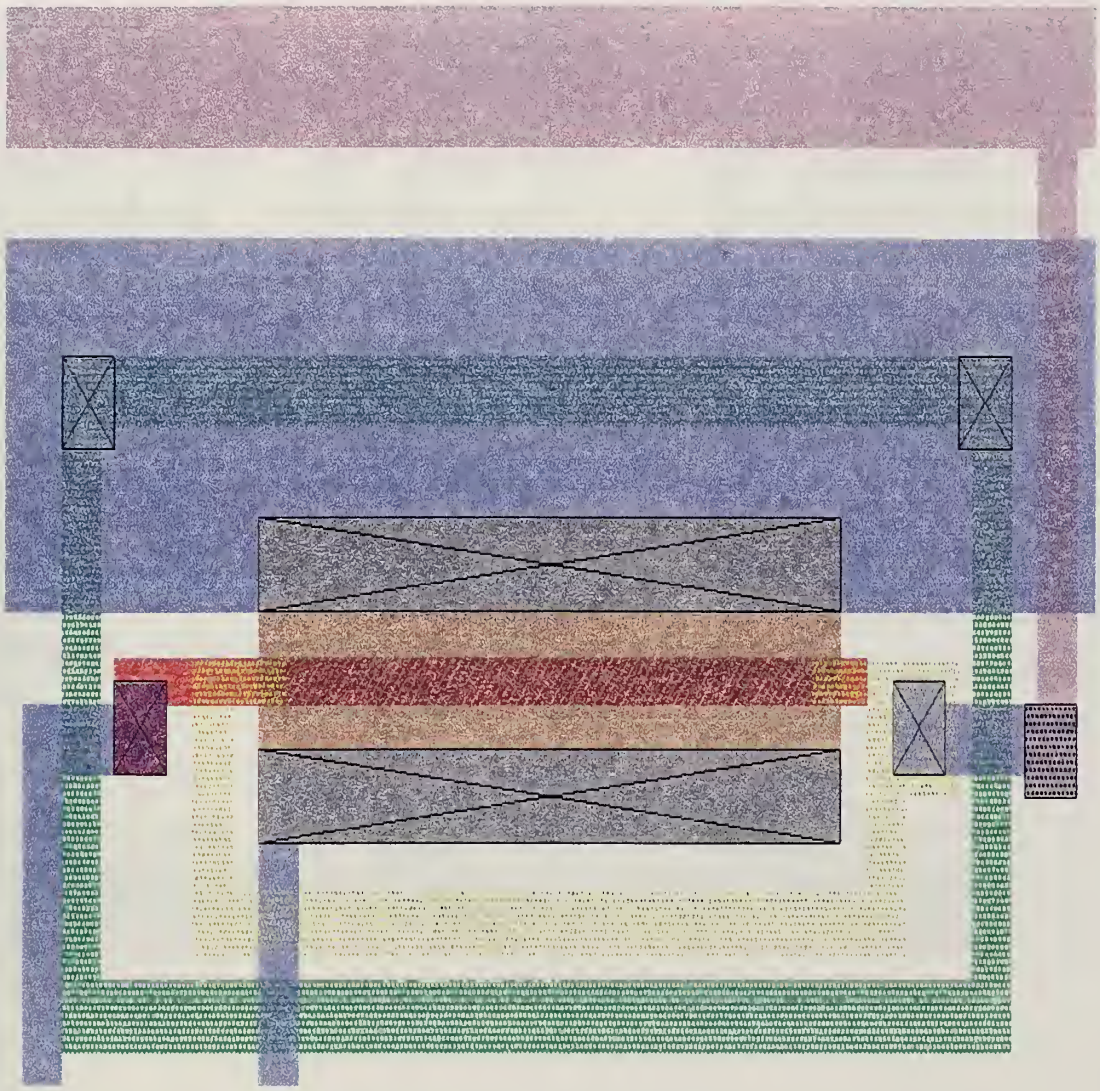


Figure B.8. Device 1P31.

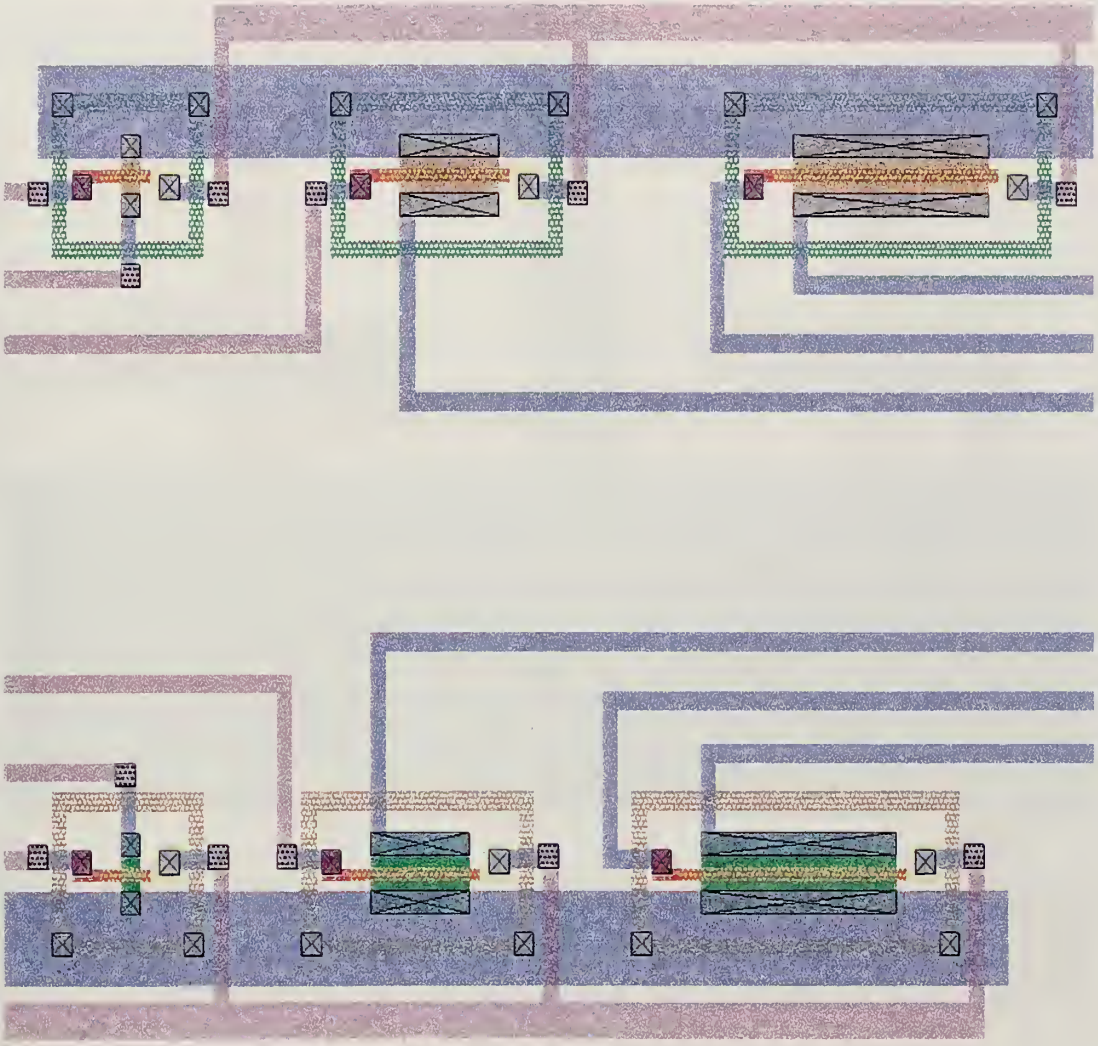


Figure B.9. Chip One Structure Two.

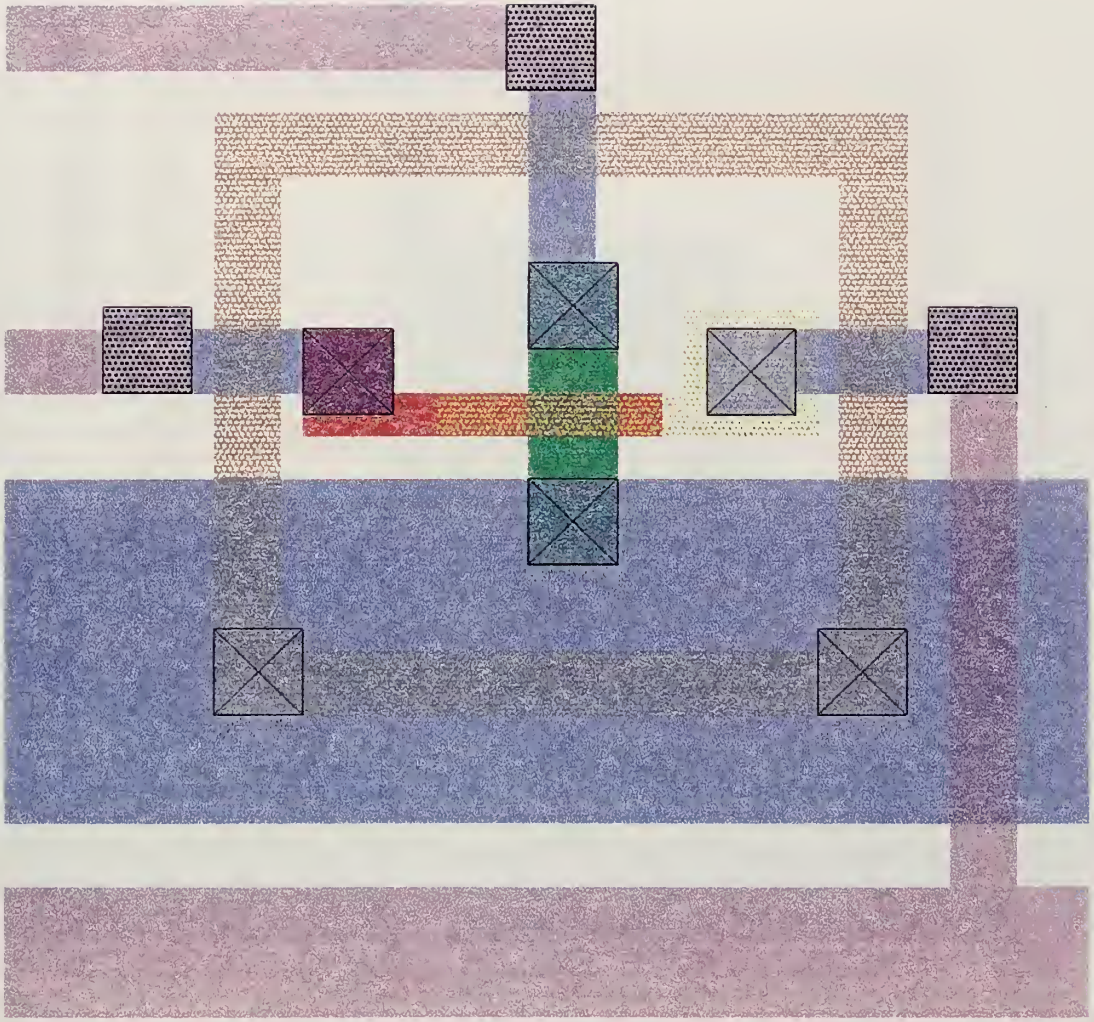


Figure B.10. Device 1N12.

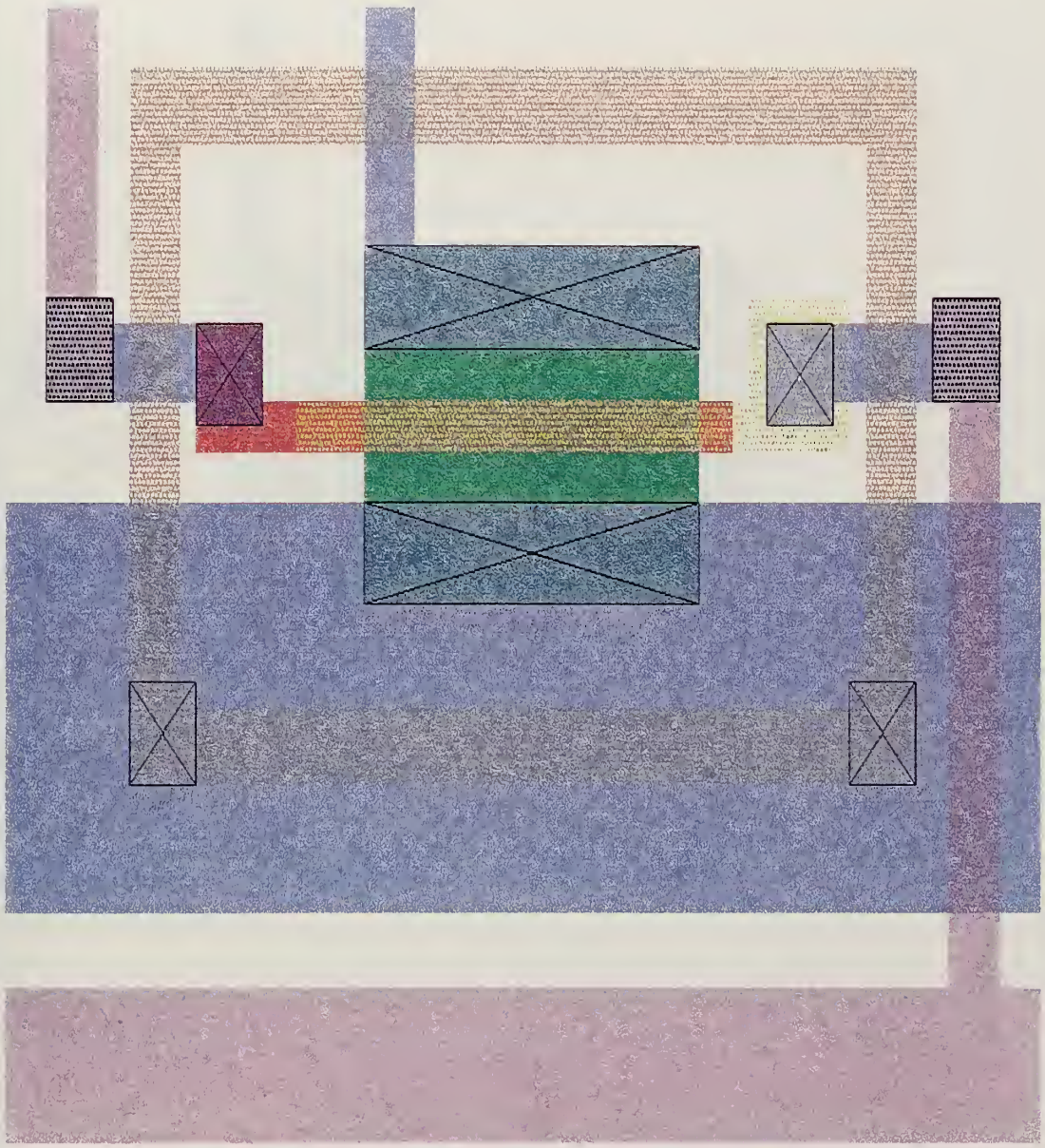


Figure B.11. Device 1N22.

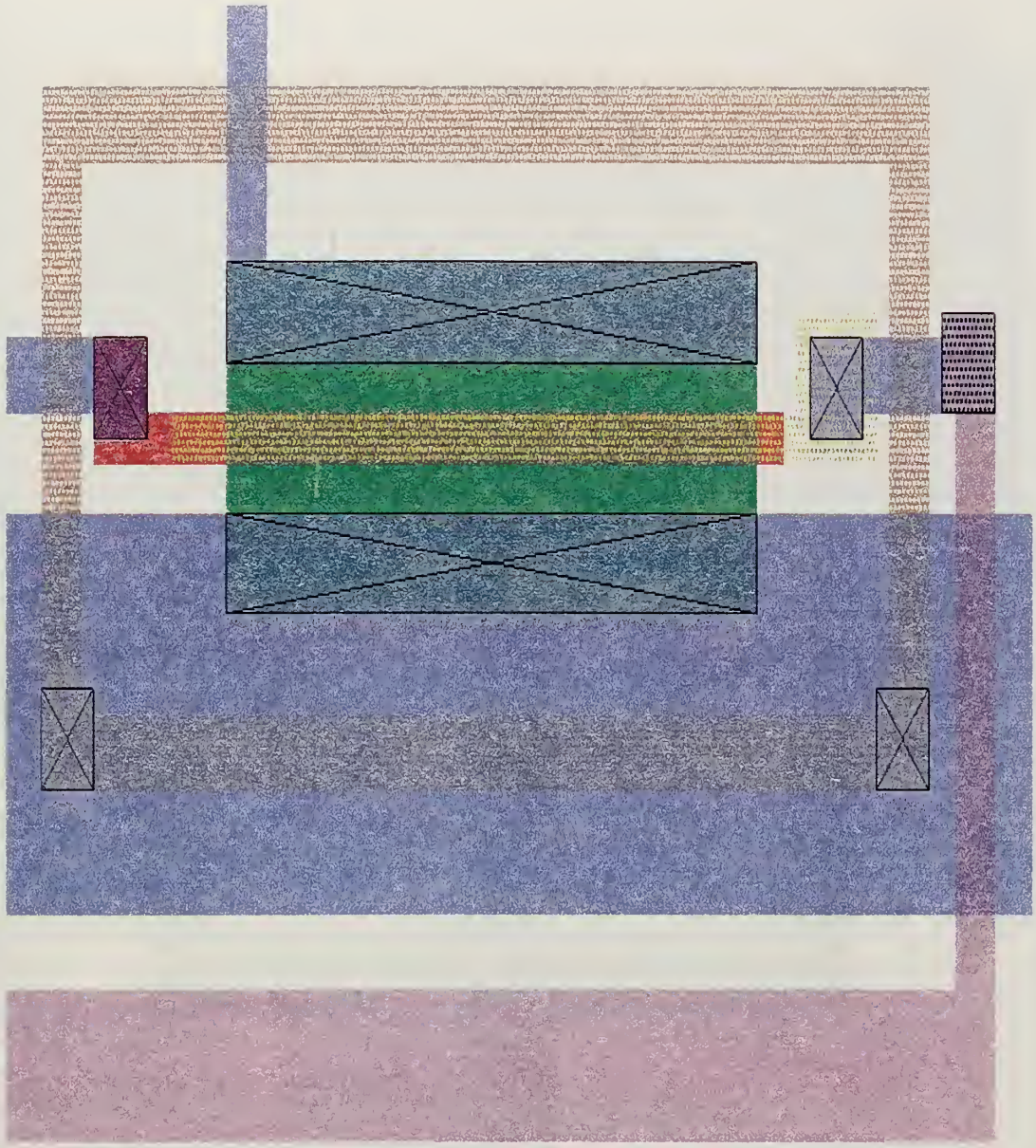


Figure B.12. Device 1N32.

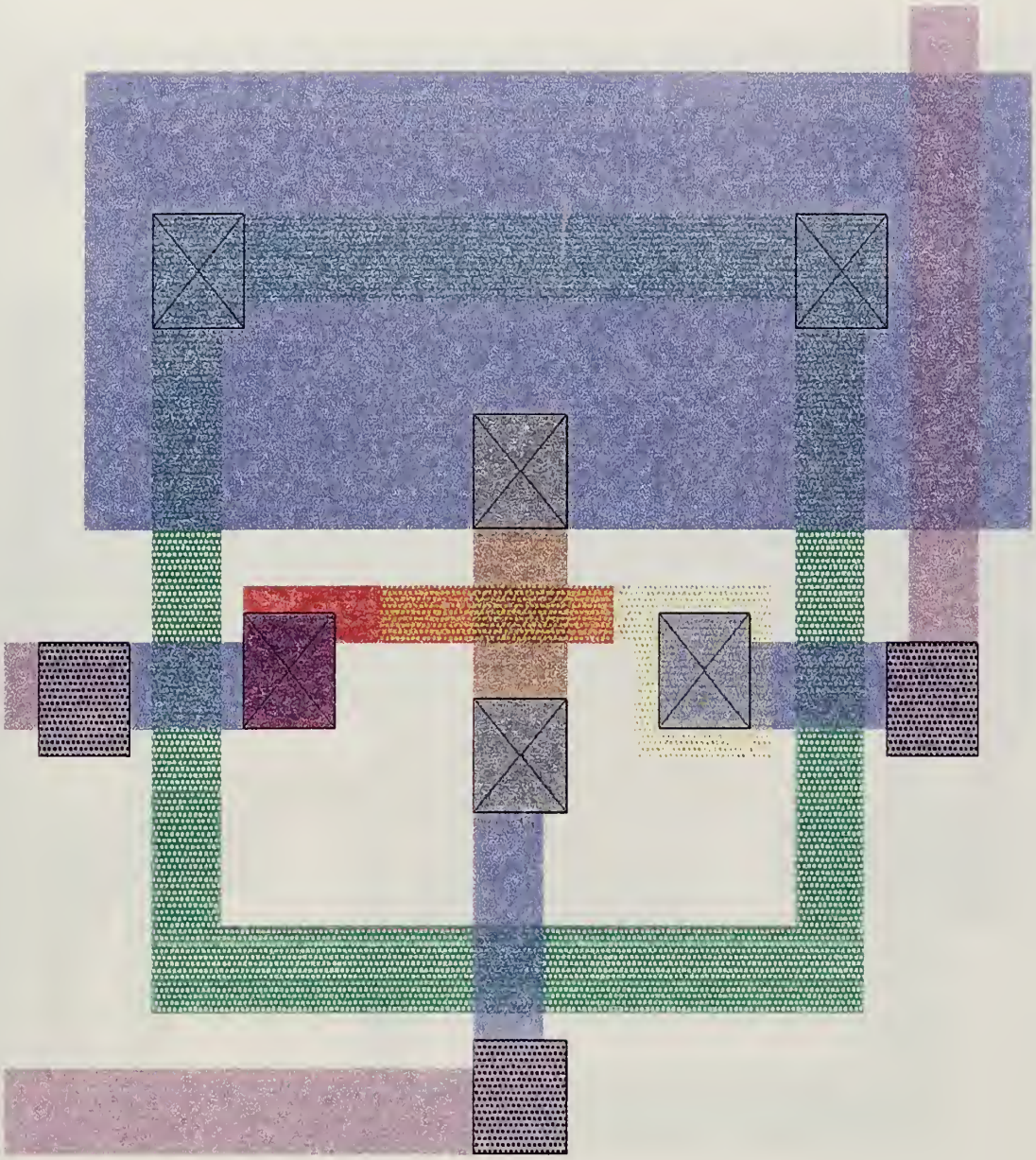


Figure B.13. Device 1P12.

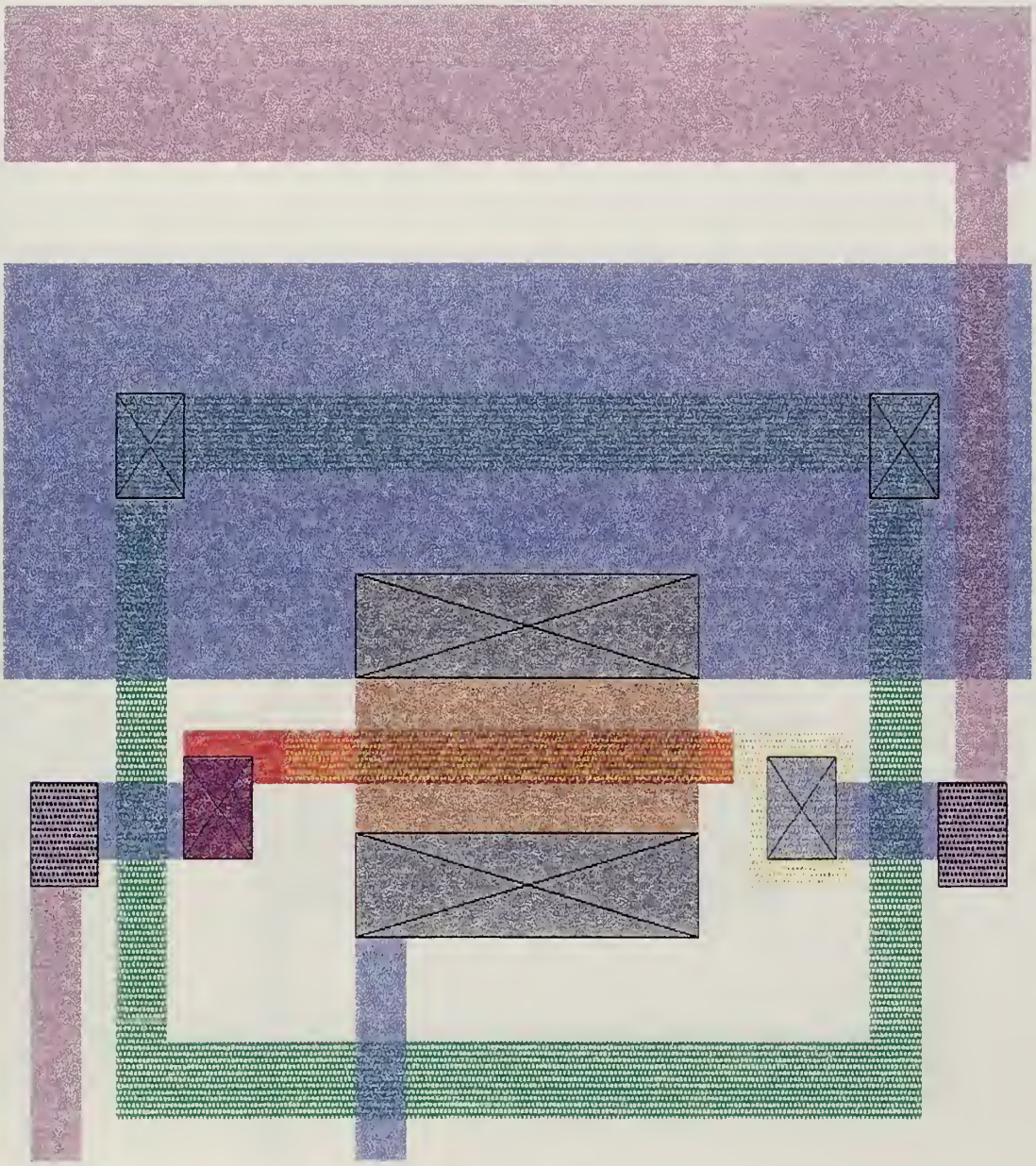


Figure B.14. Device 1P22.

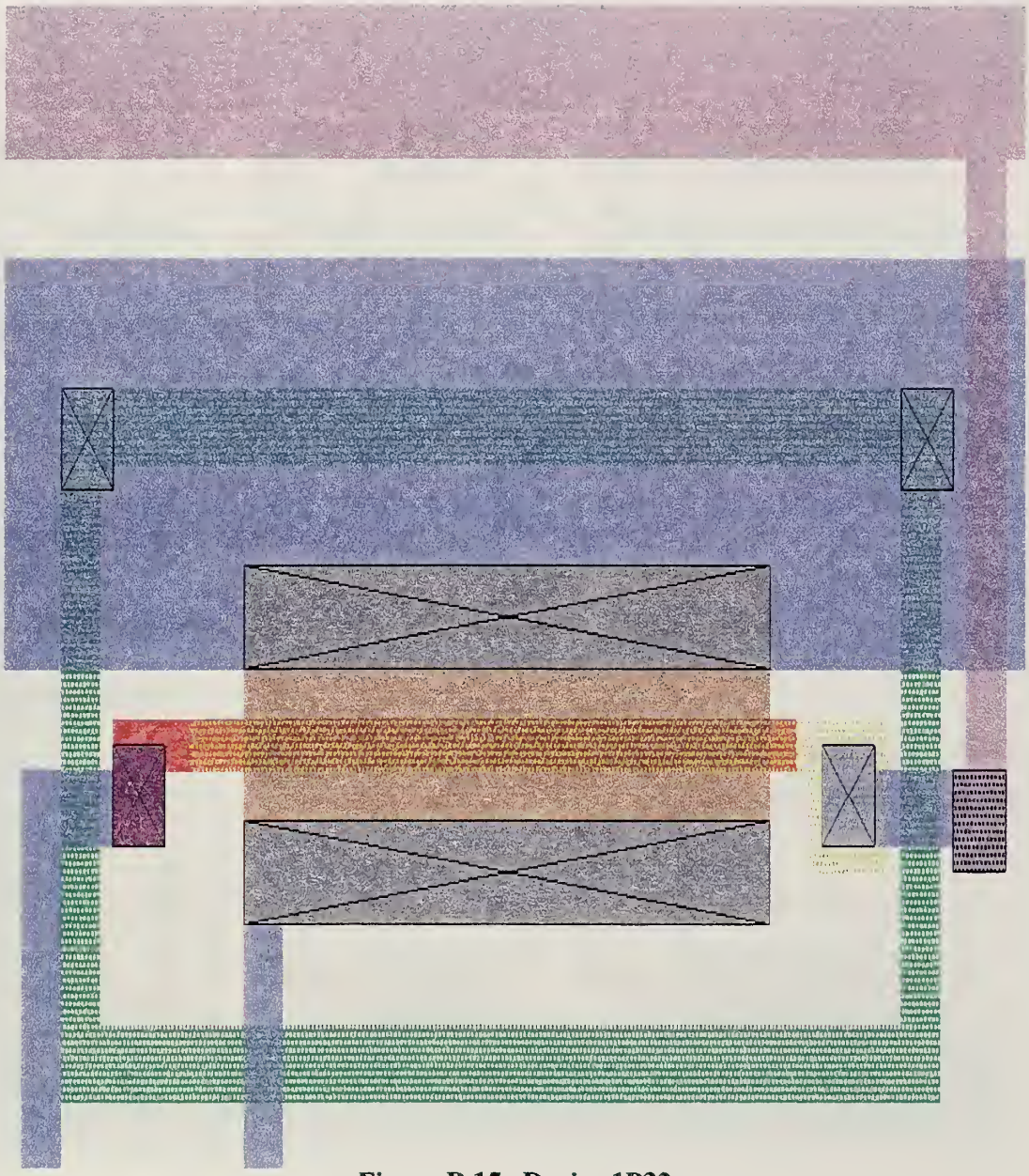


Figure B.15. Device 1P32.

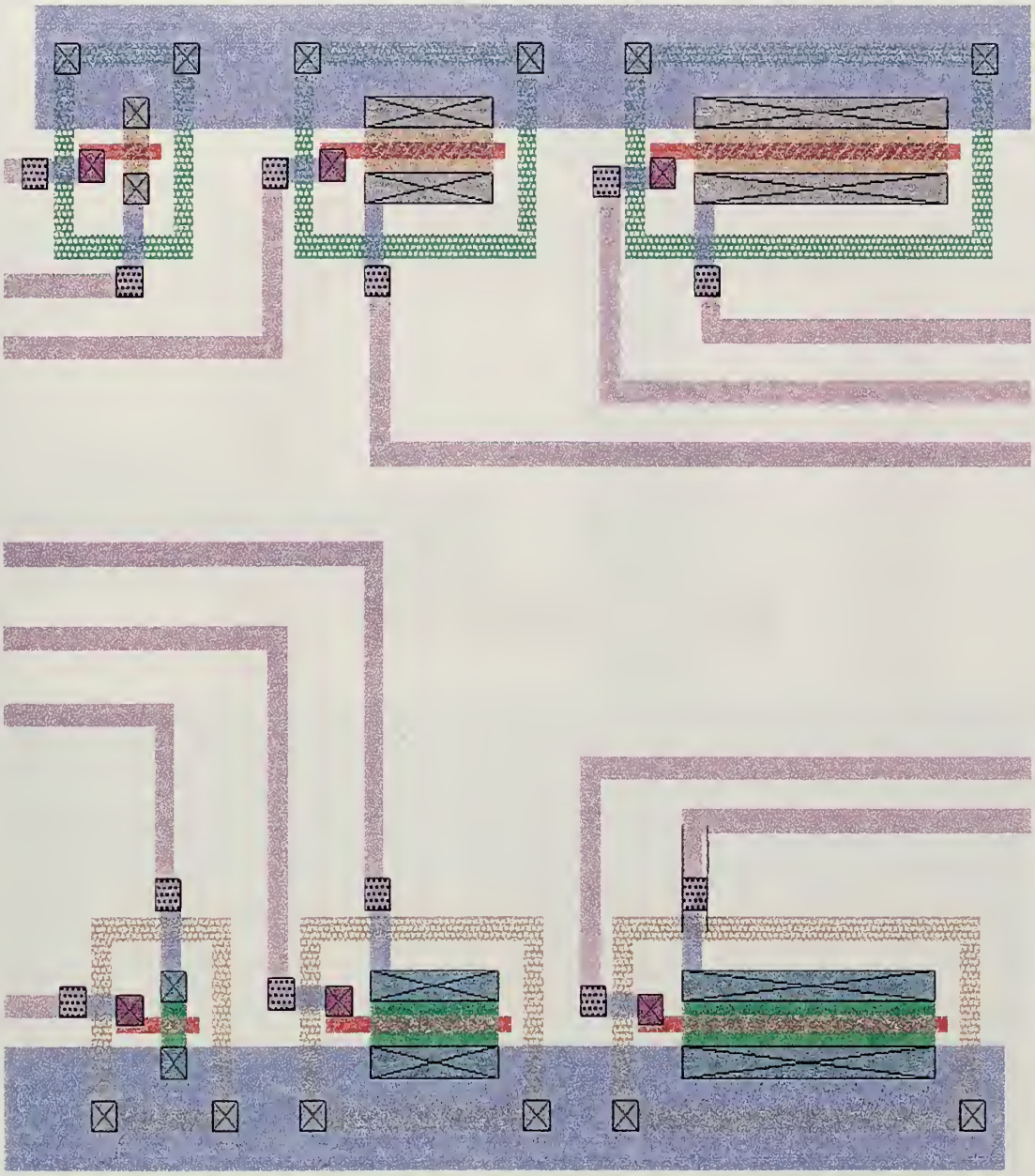


Figure B.16. Chip One Structure Three.

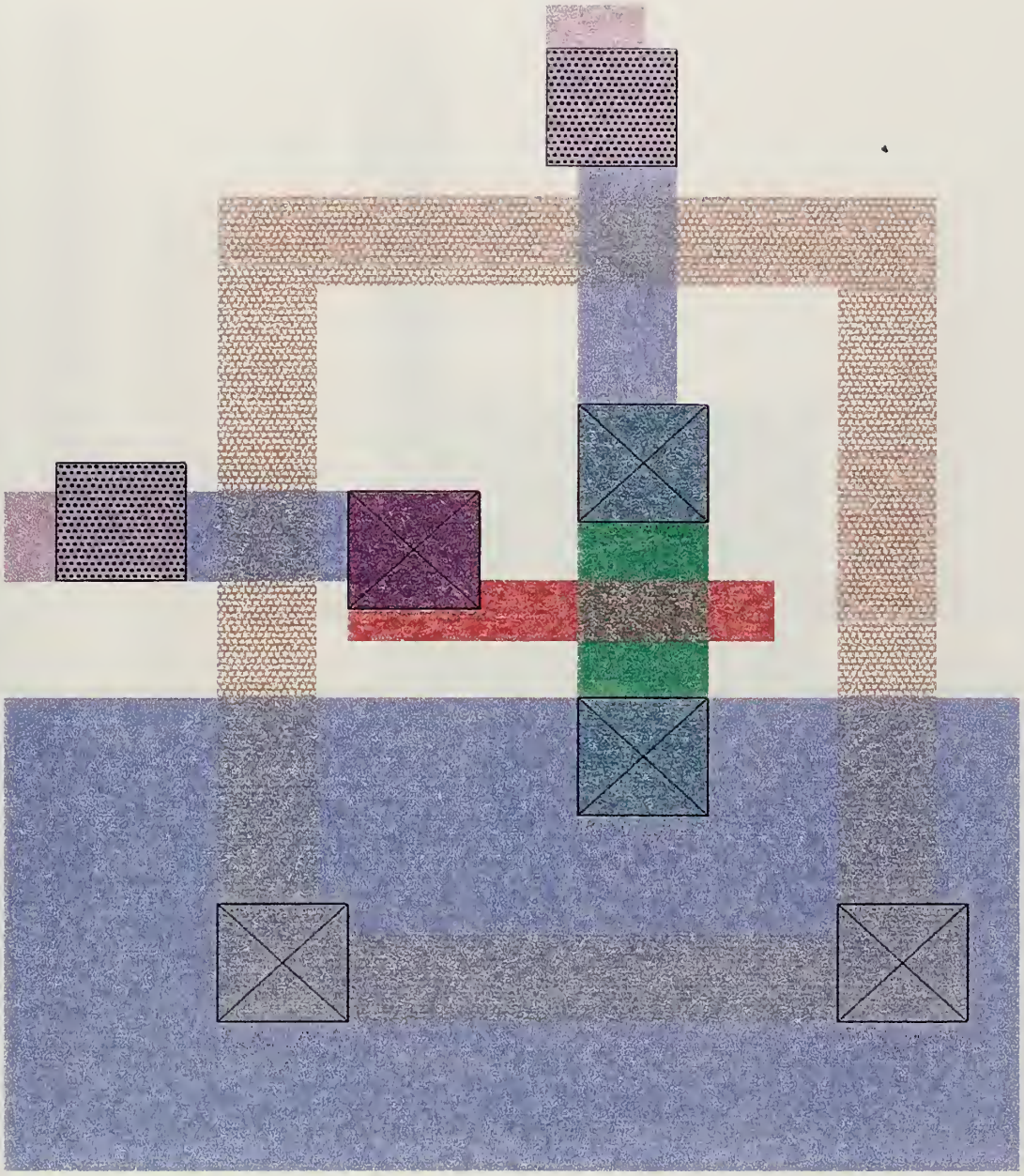


Figure B.17. Device 1N13.

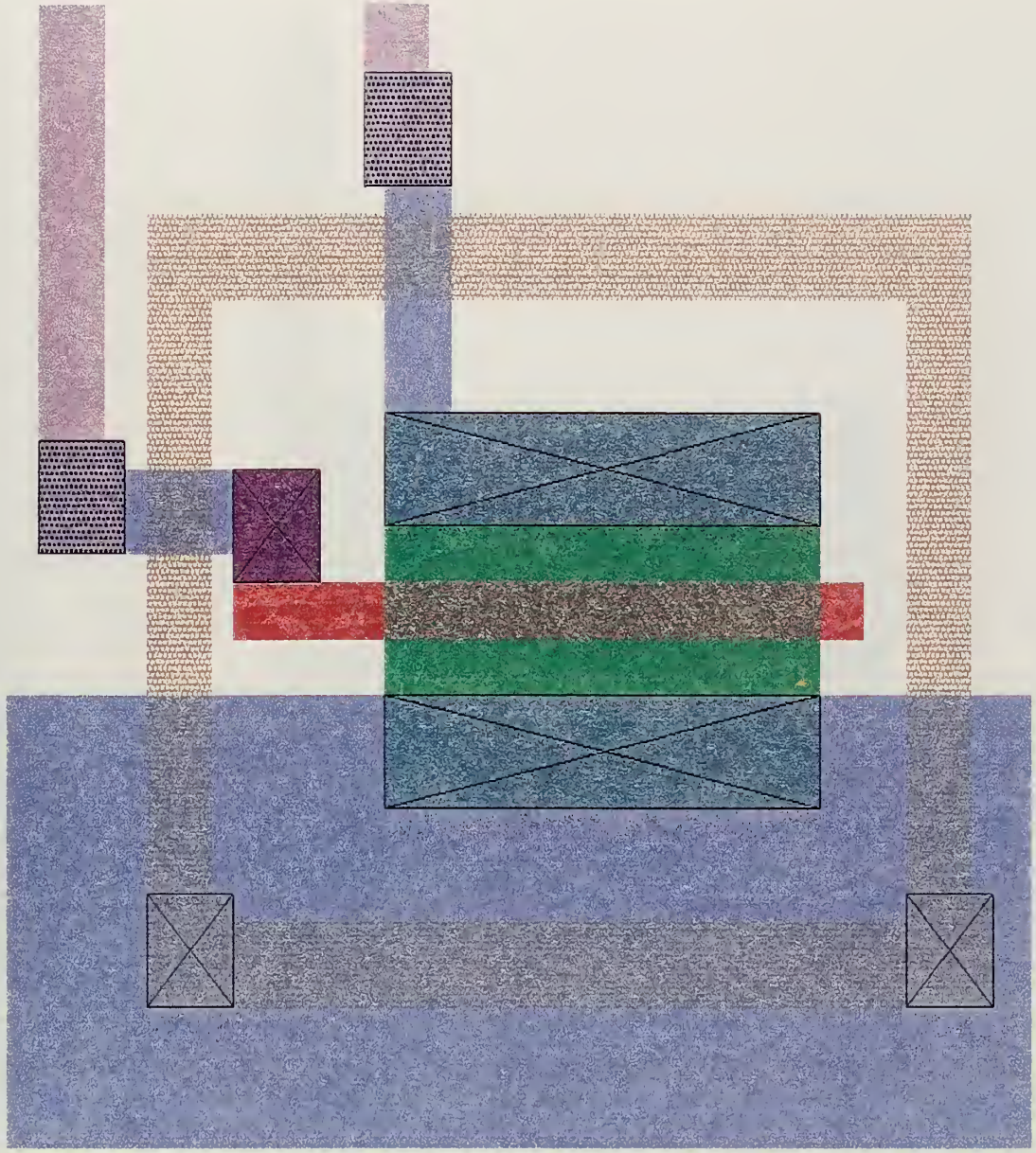


Figure B.18. Device 1N23.

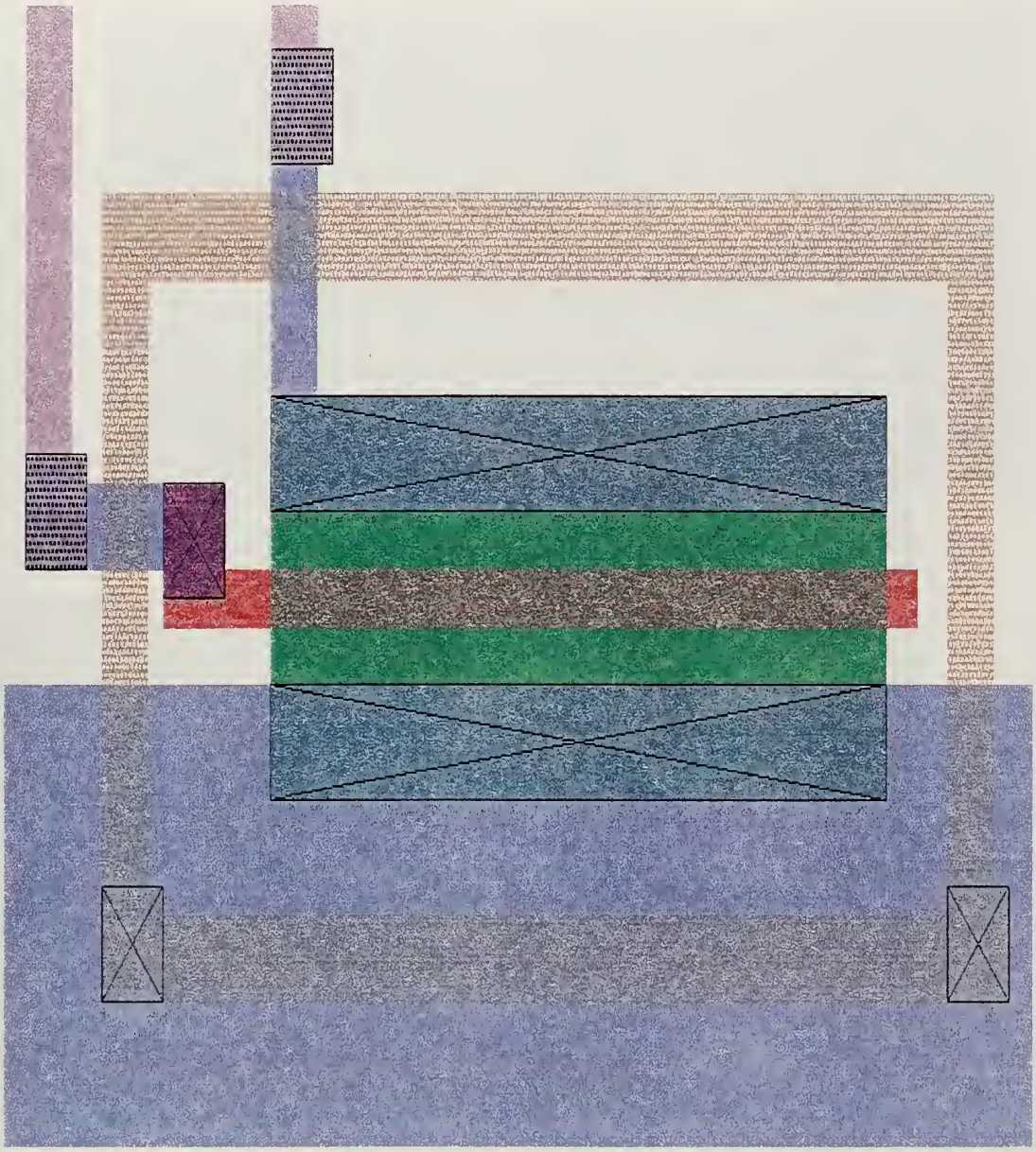


Figure B.19. Device 1N33.

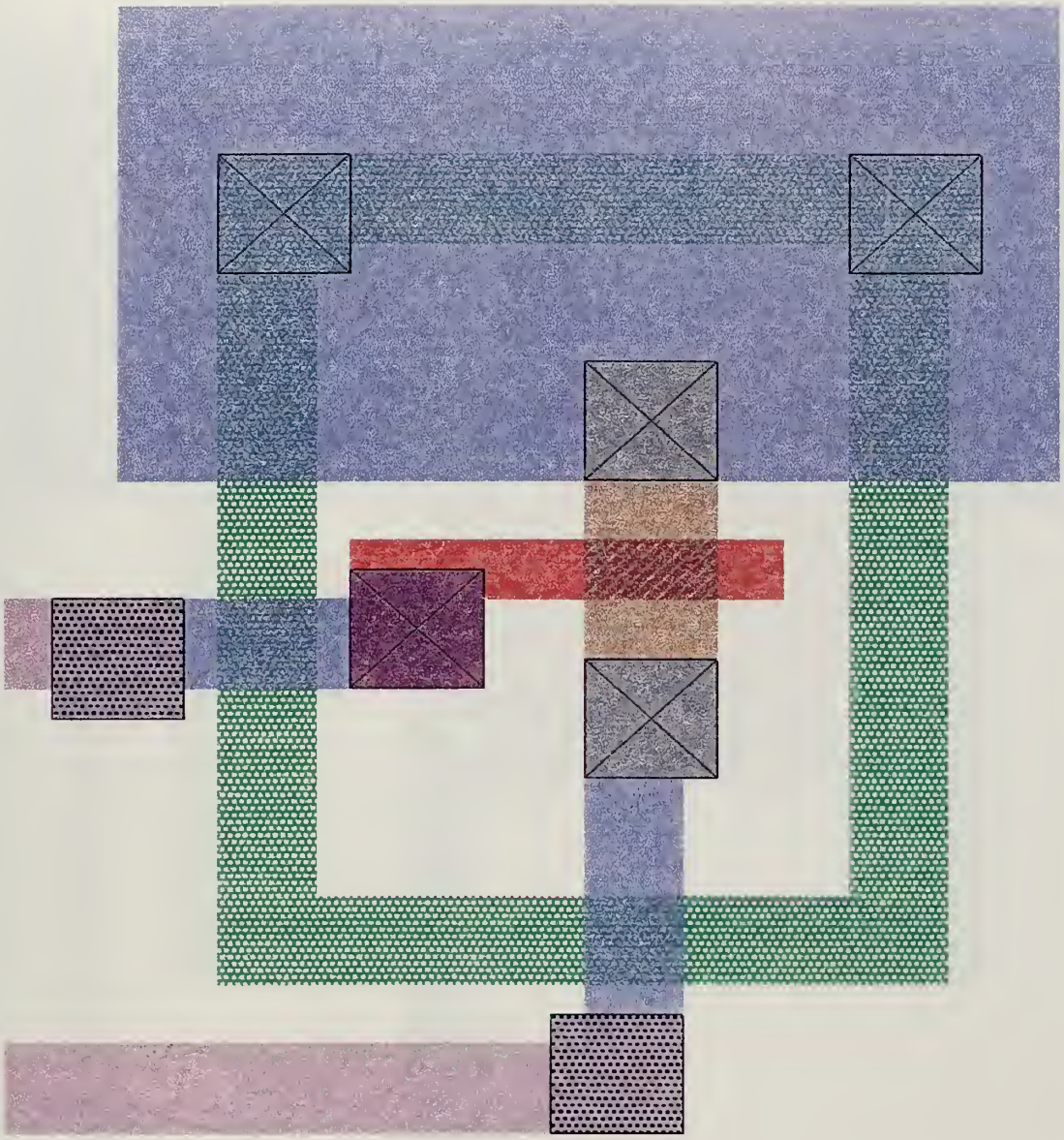


Figure B.20. Device 1P13.

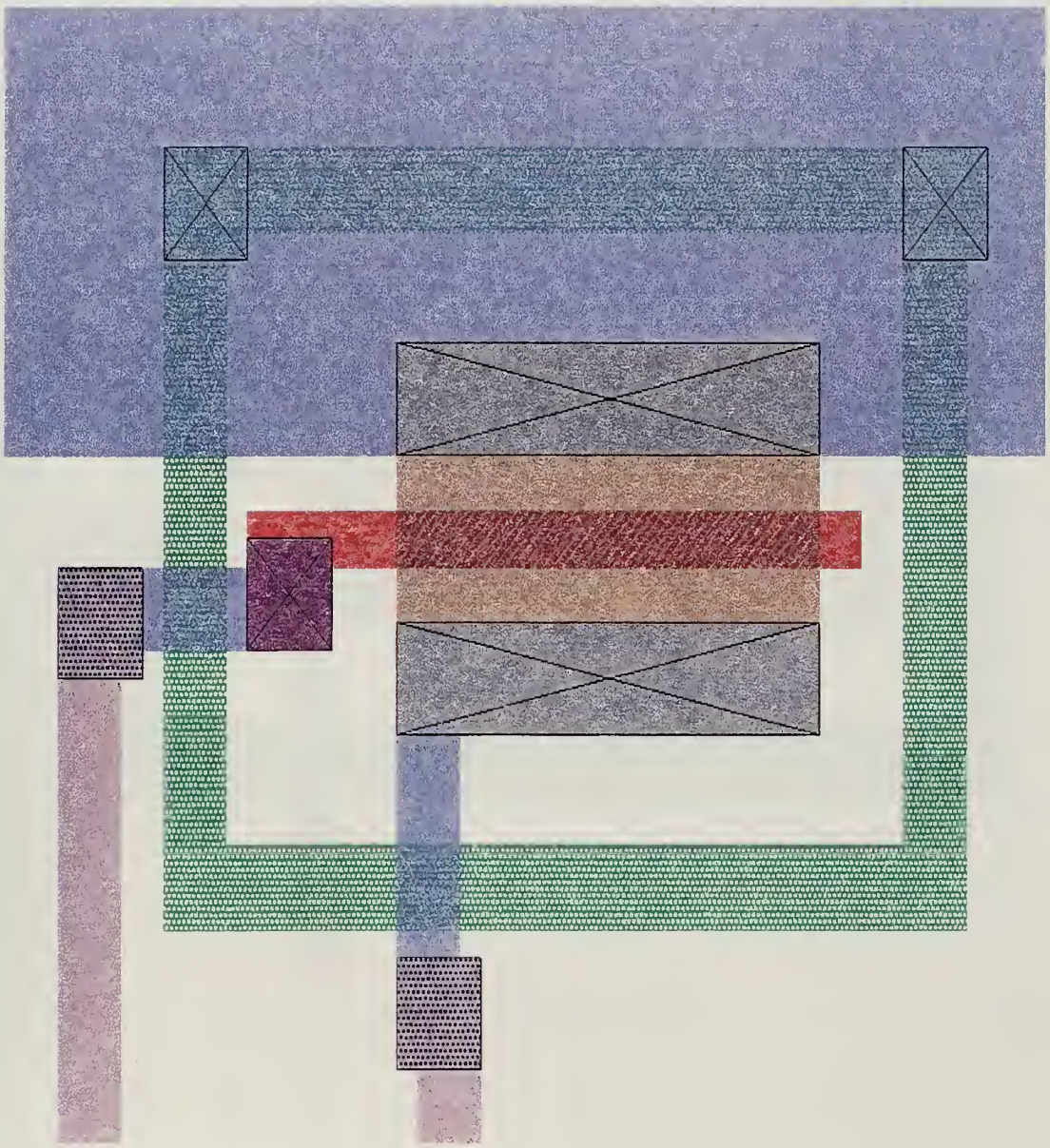


Figure B.21. Device 1P23.

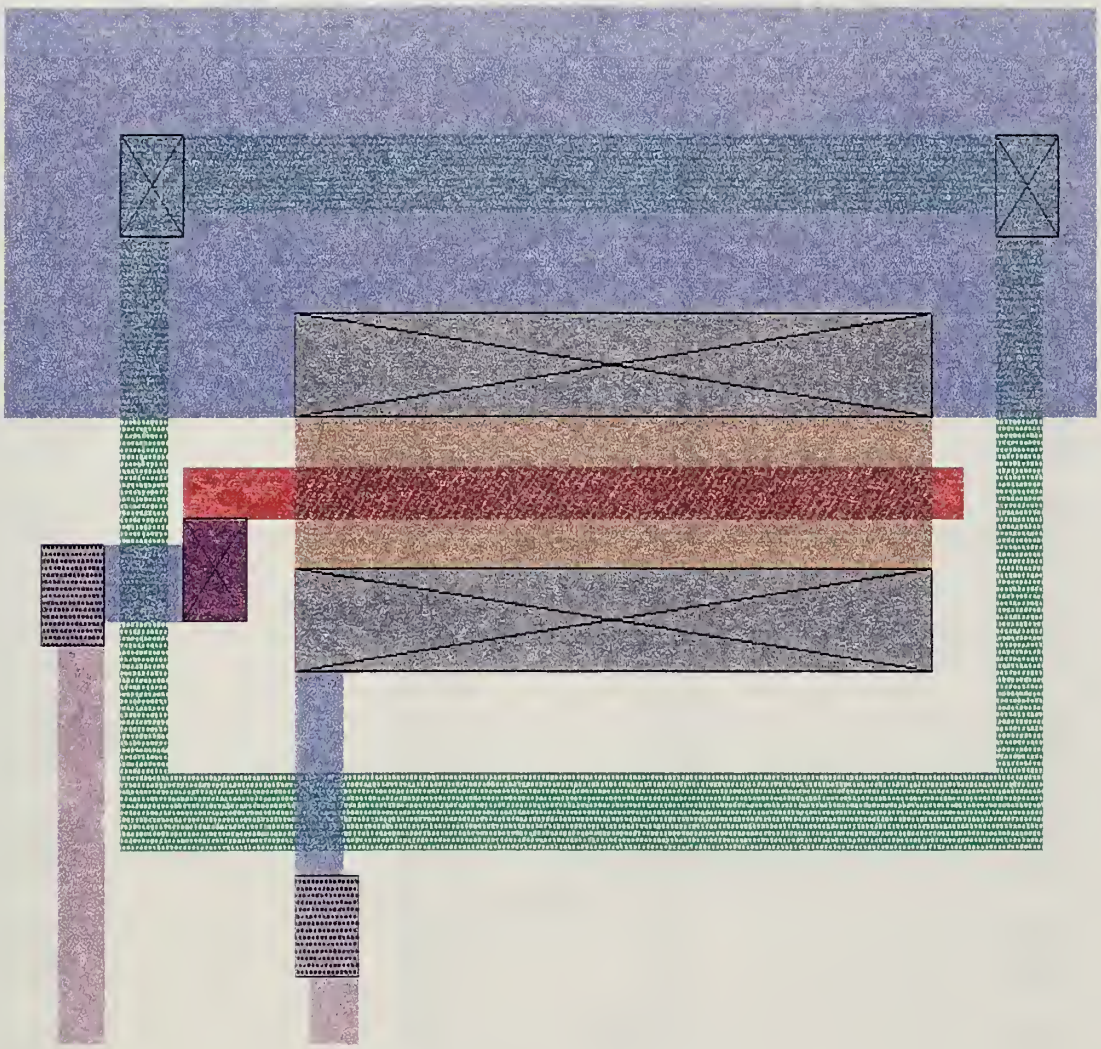


Figure B.22. Device 1P33.

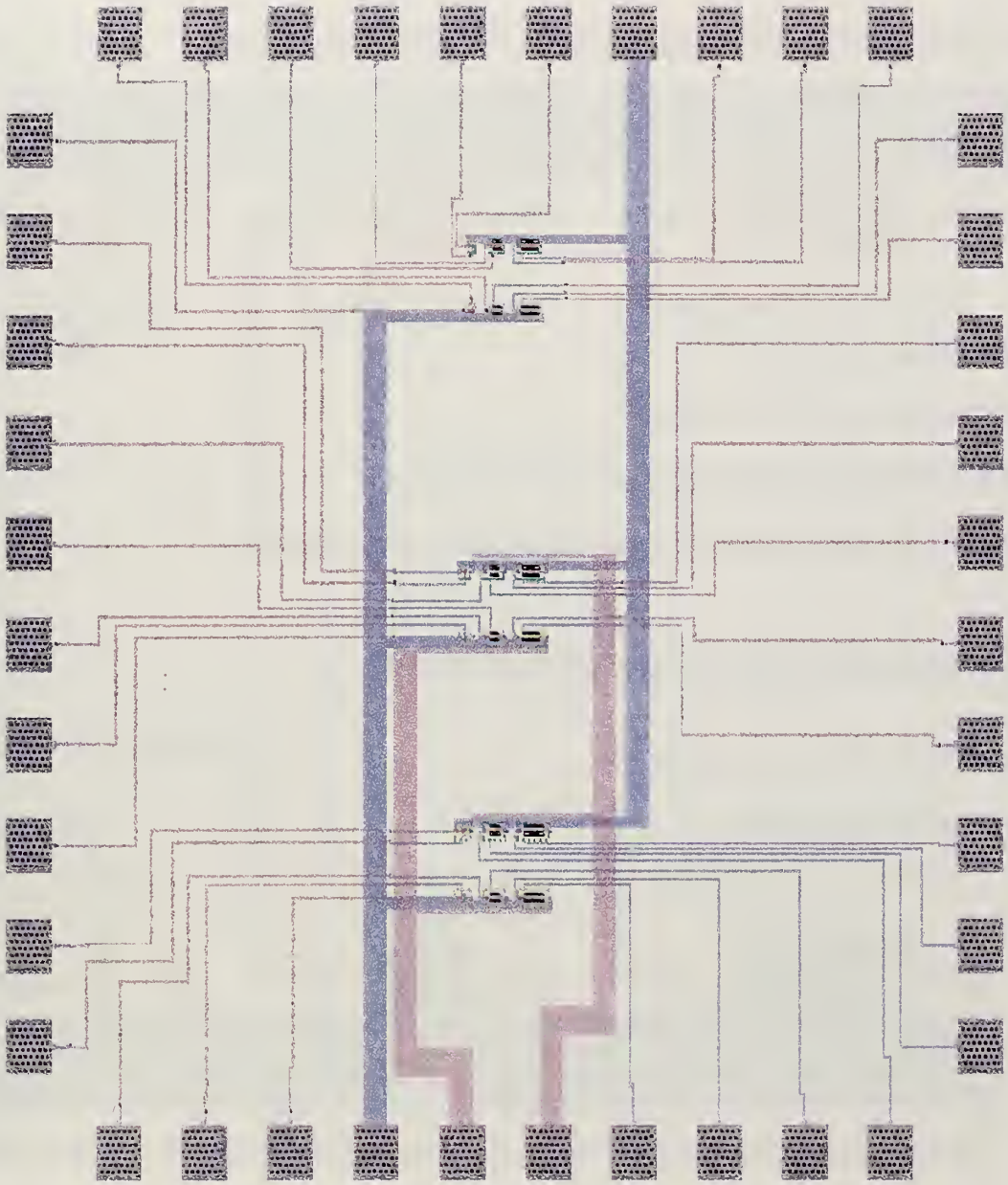


Figure B.23. Chip Two.

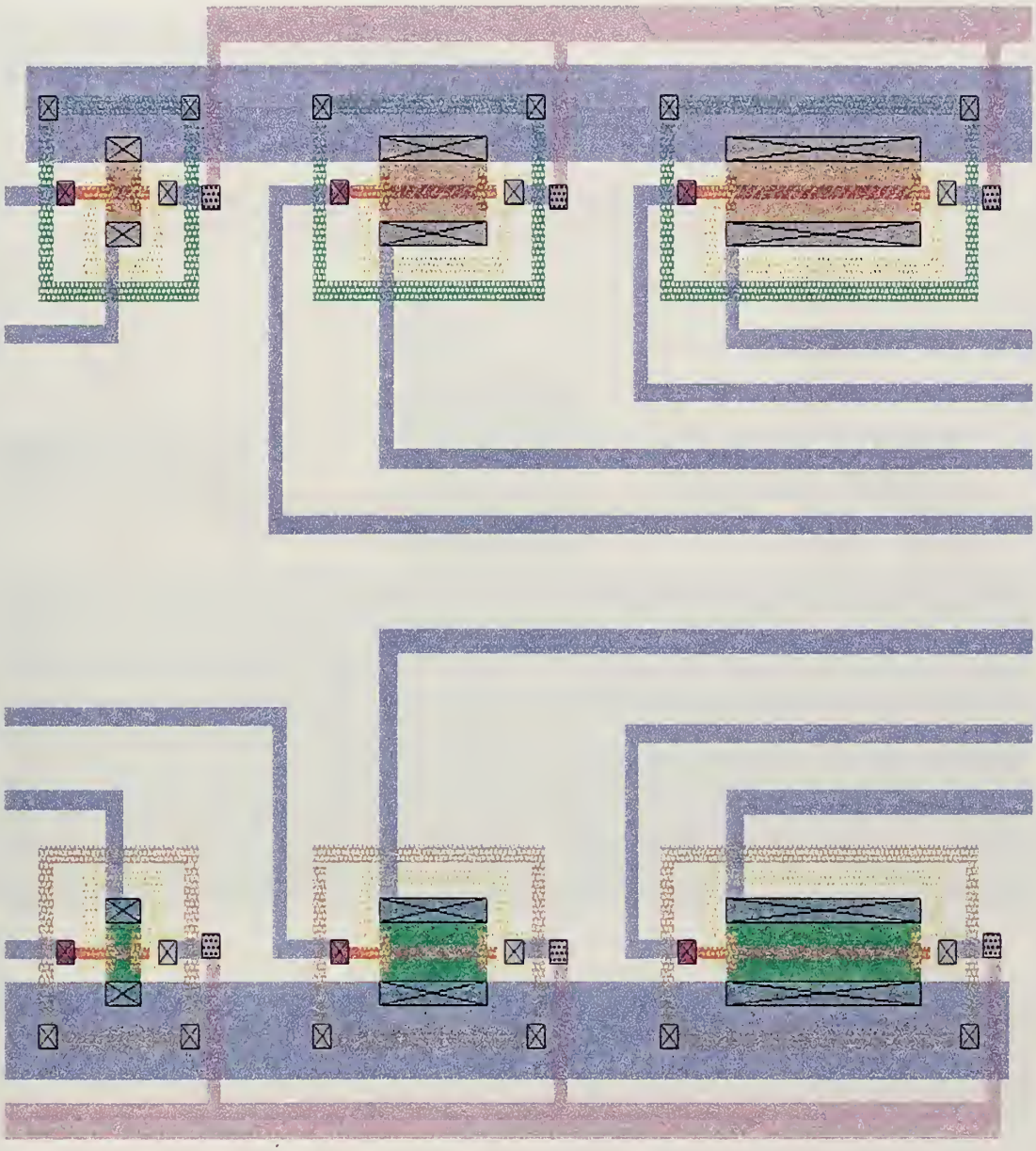


Figure B.24. Chip Two Structure One.

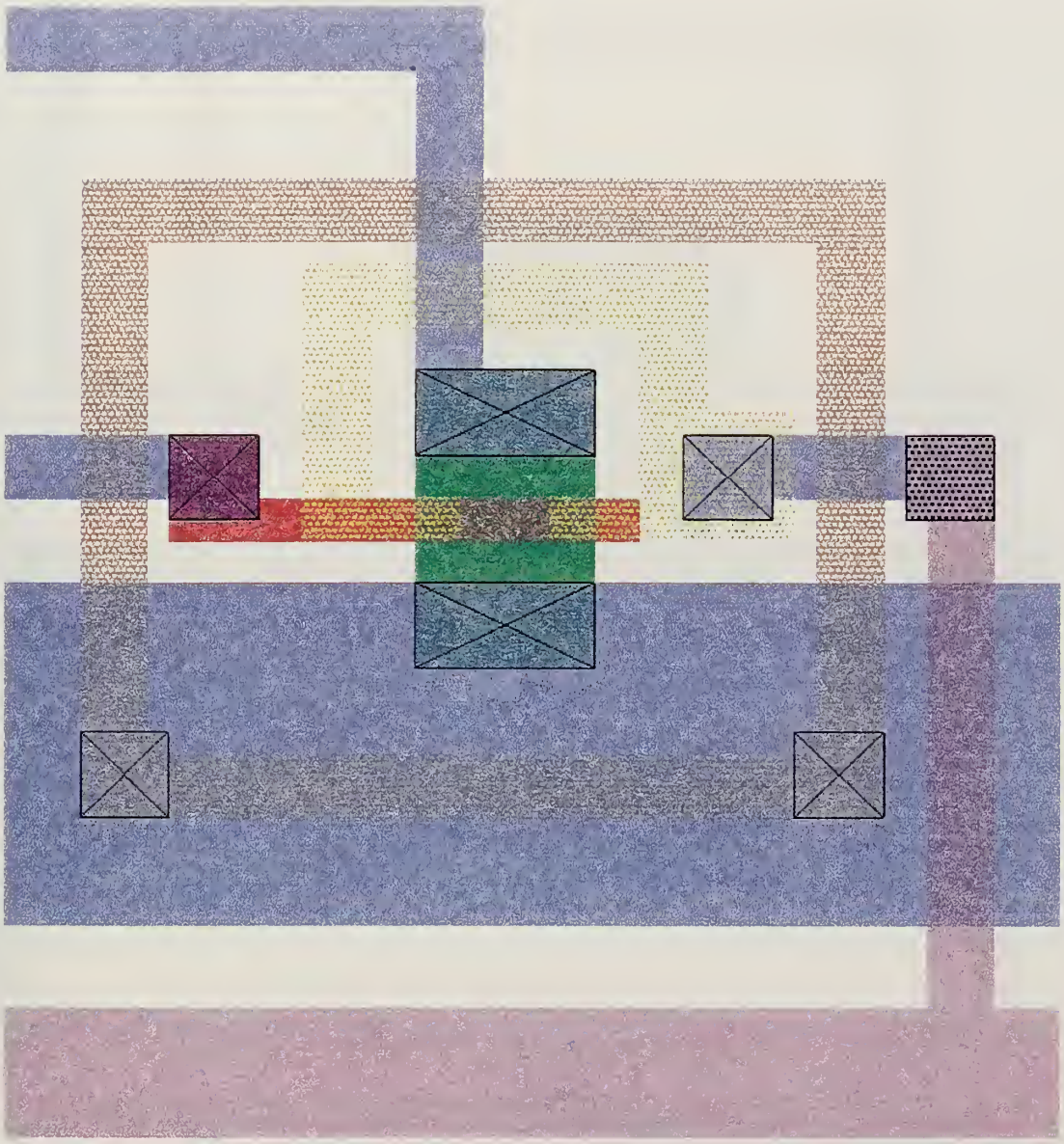


Figure B.25. Device 2N11.

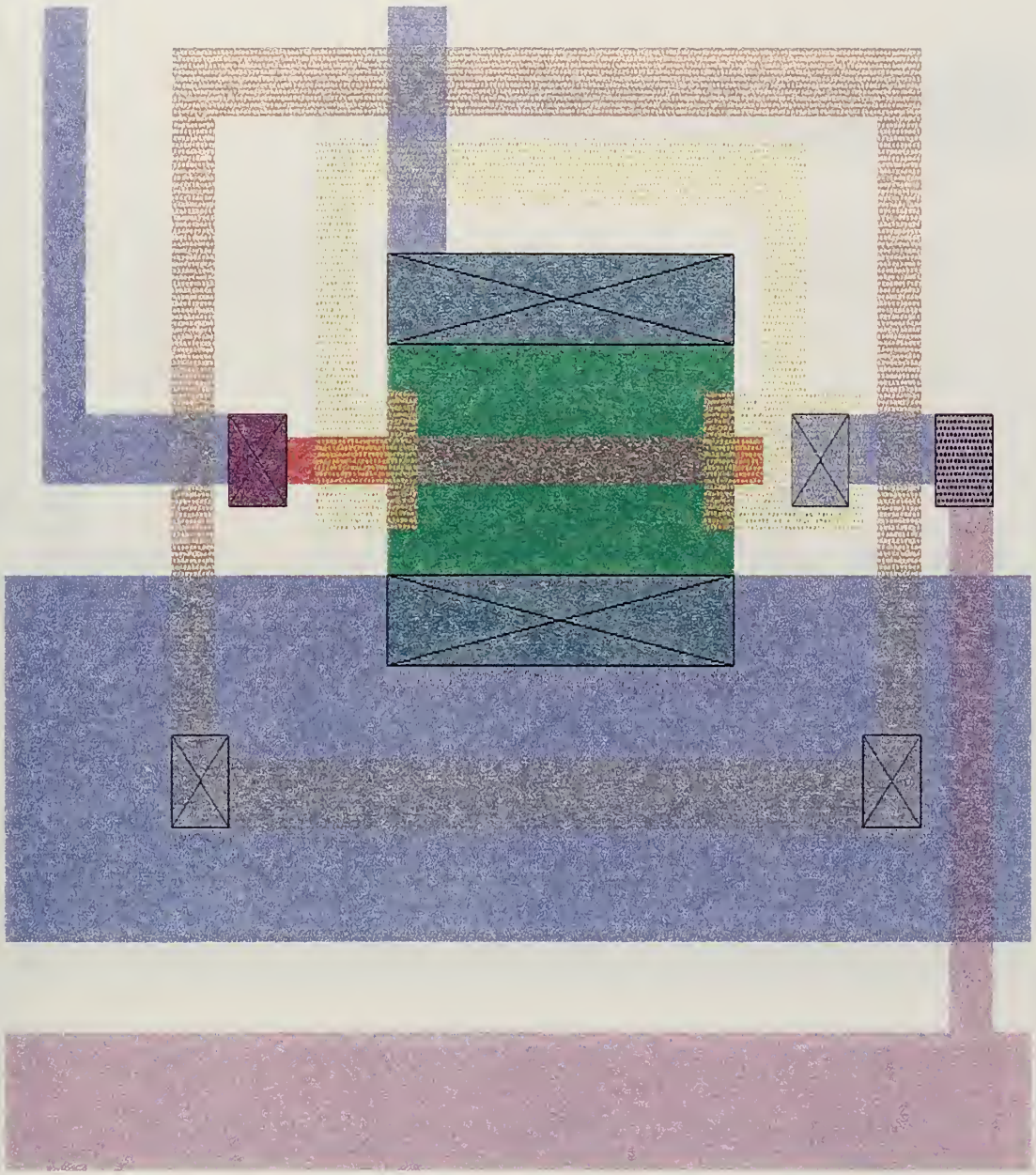


Figure B.26. Device 2N21.

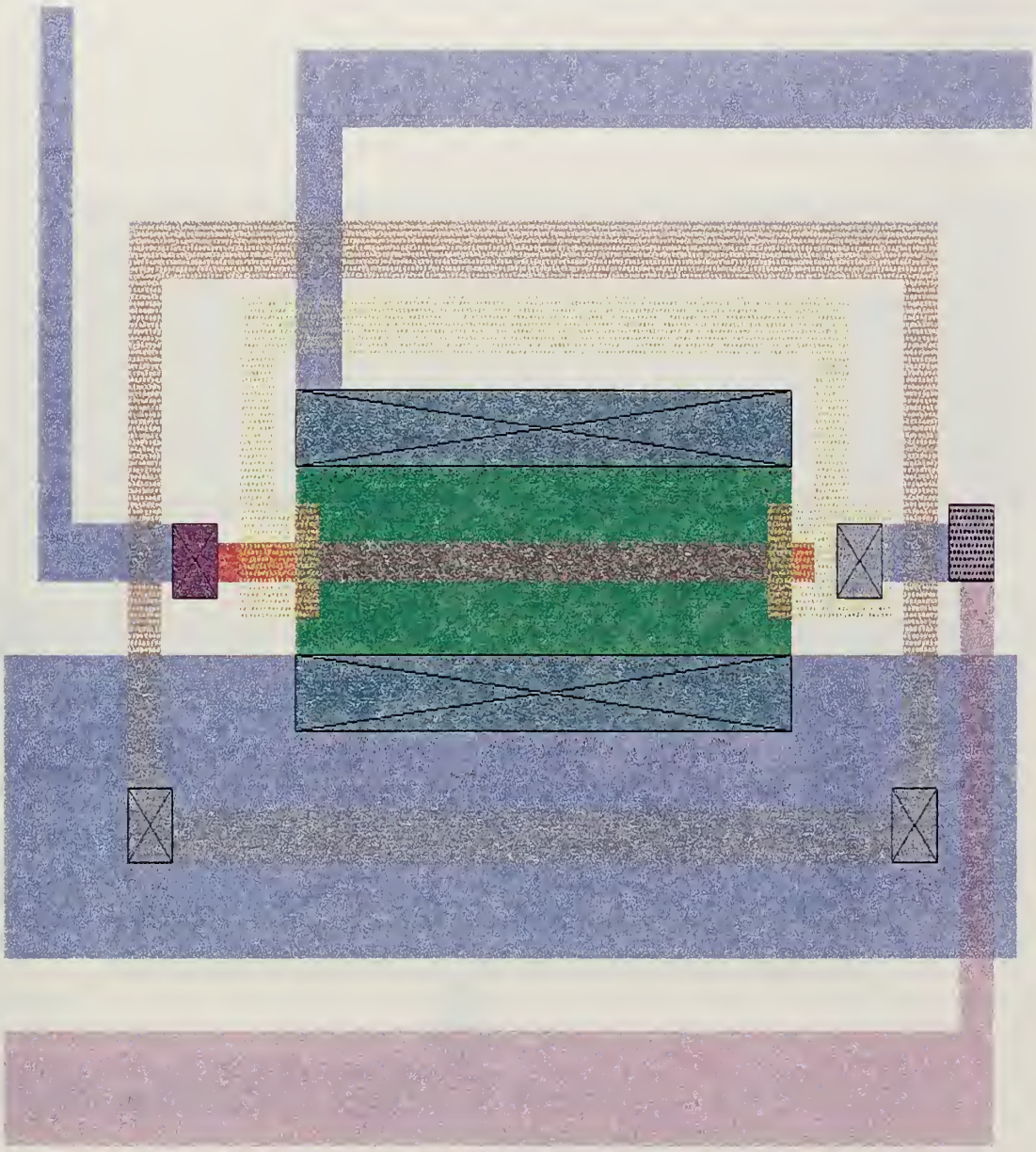


Figure B.27. Device 2N31.

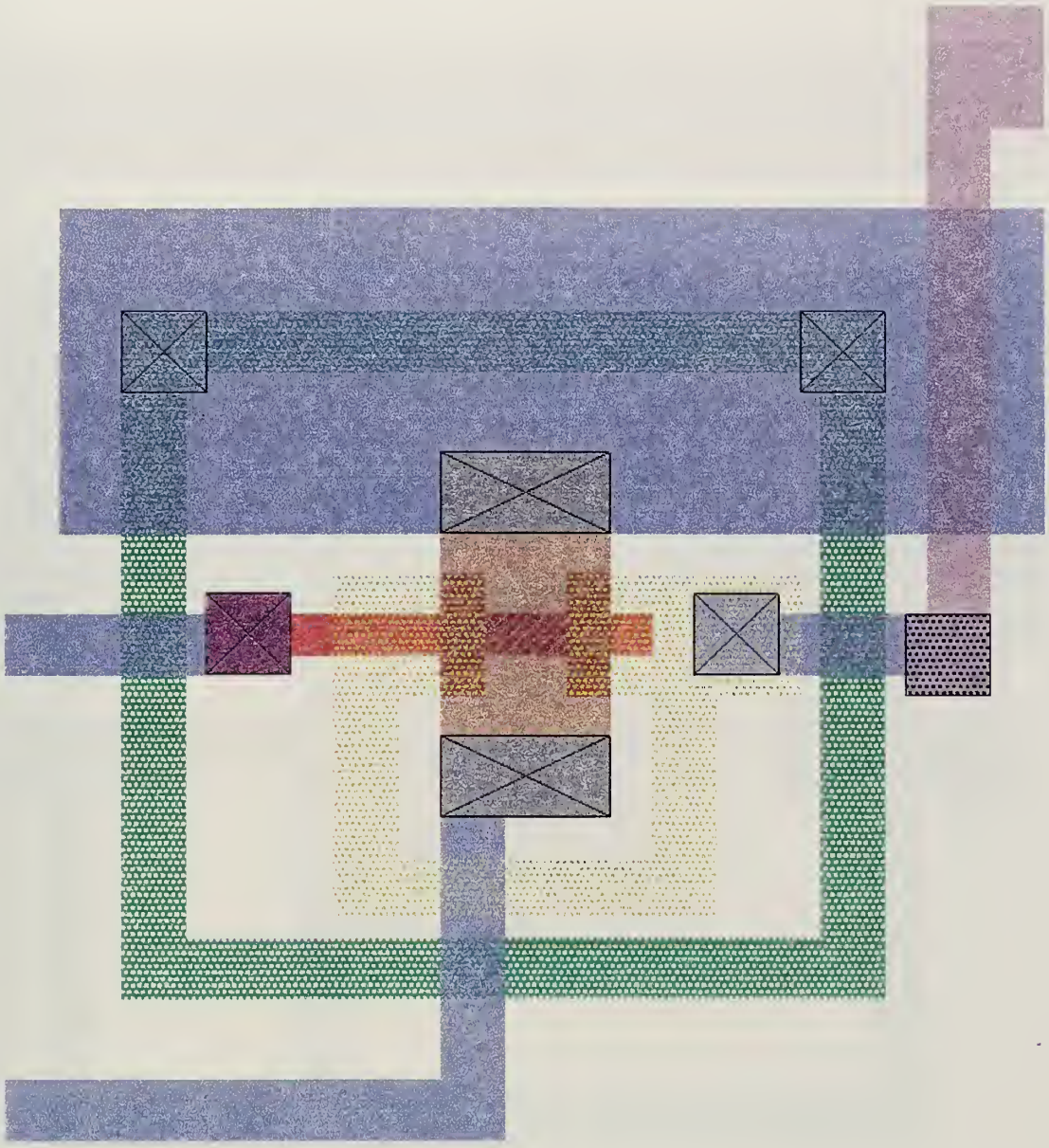


Figure B.28. Device 2P11.

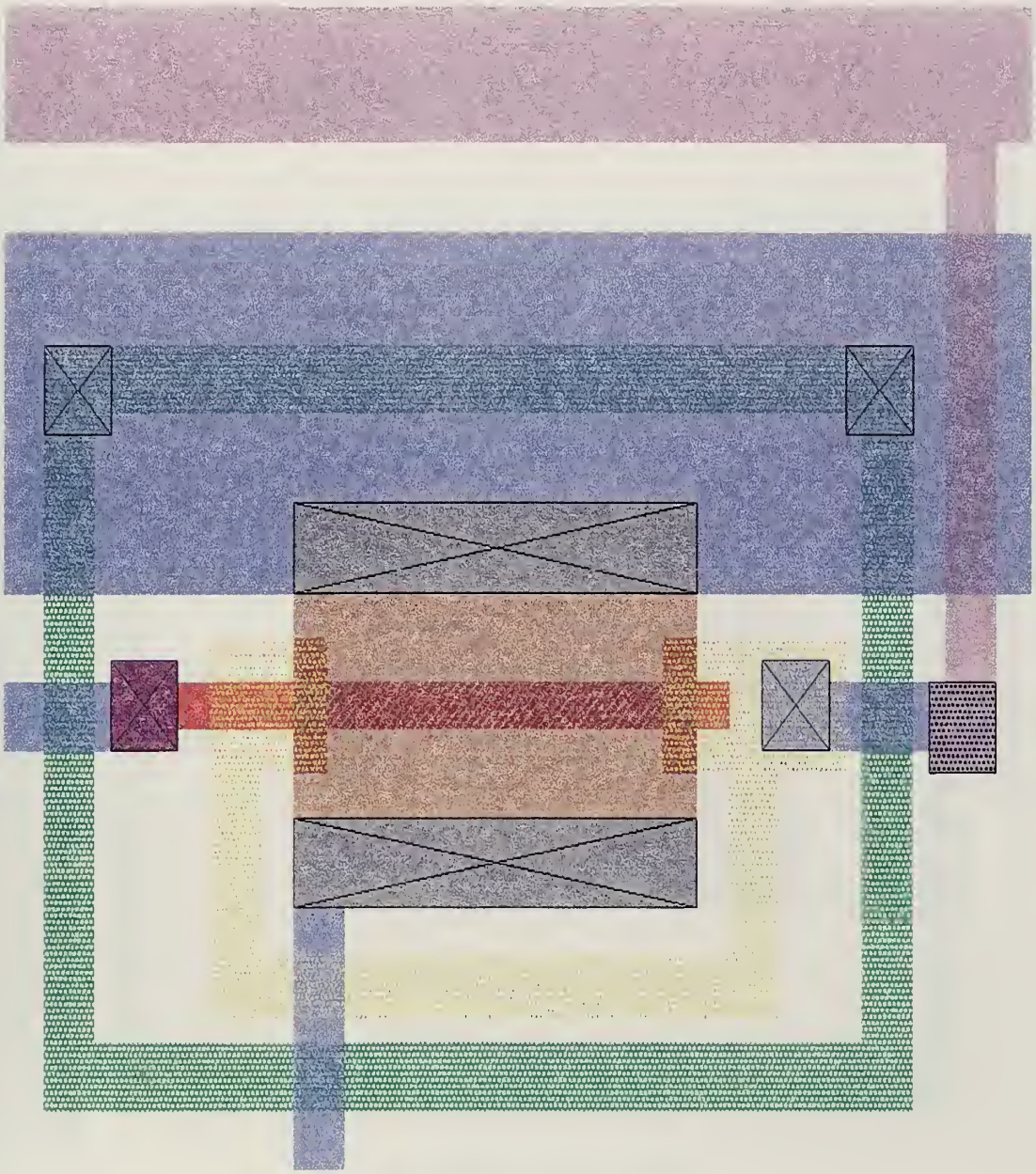


Figure B.29. Device 2P21.

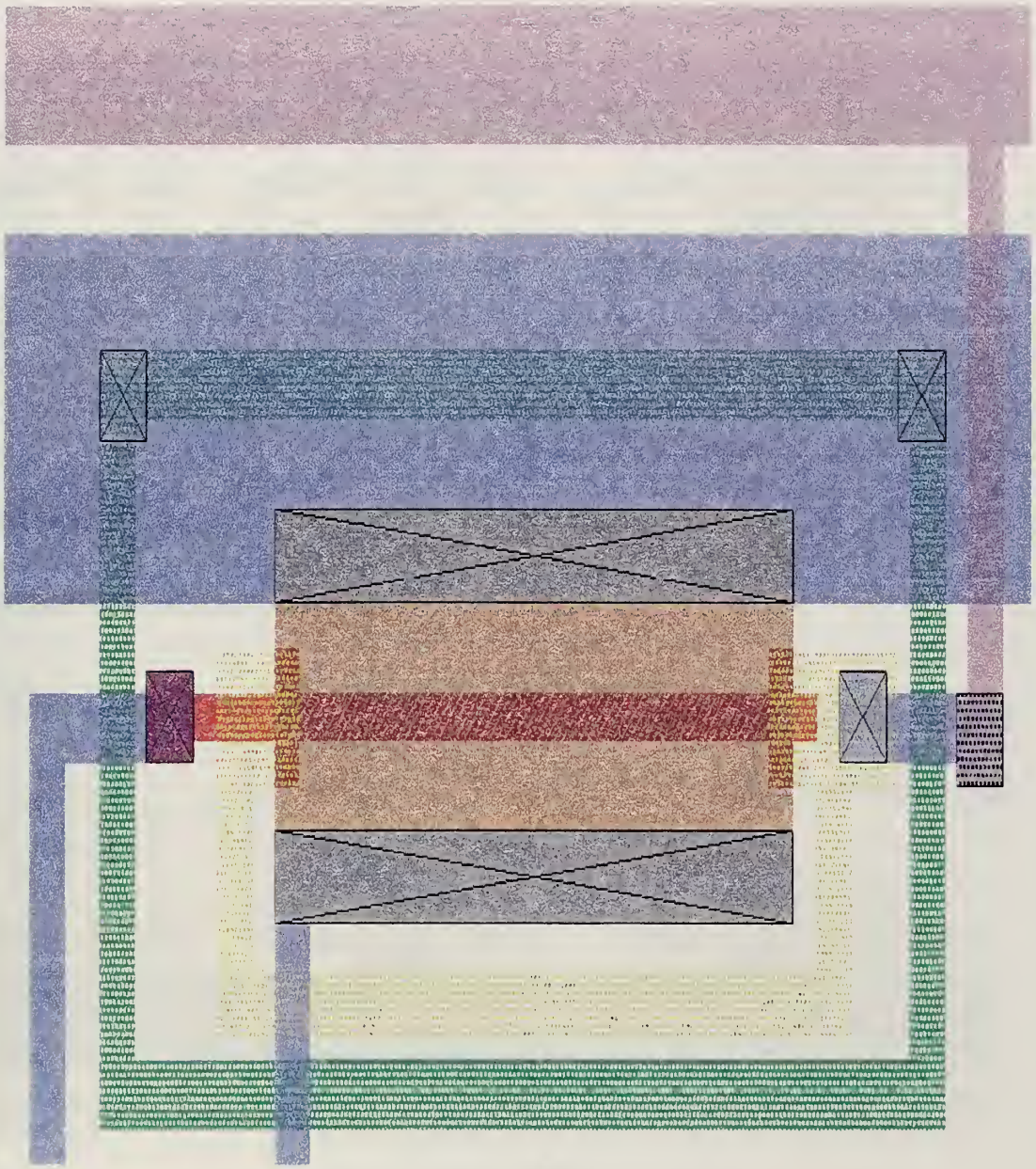


Figure B.30. Device 2P31.

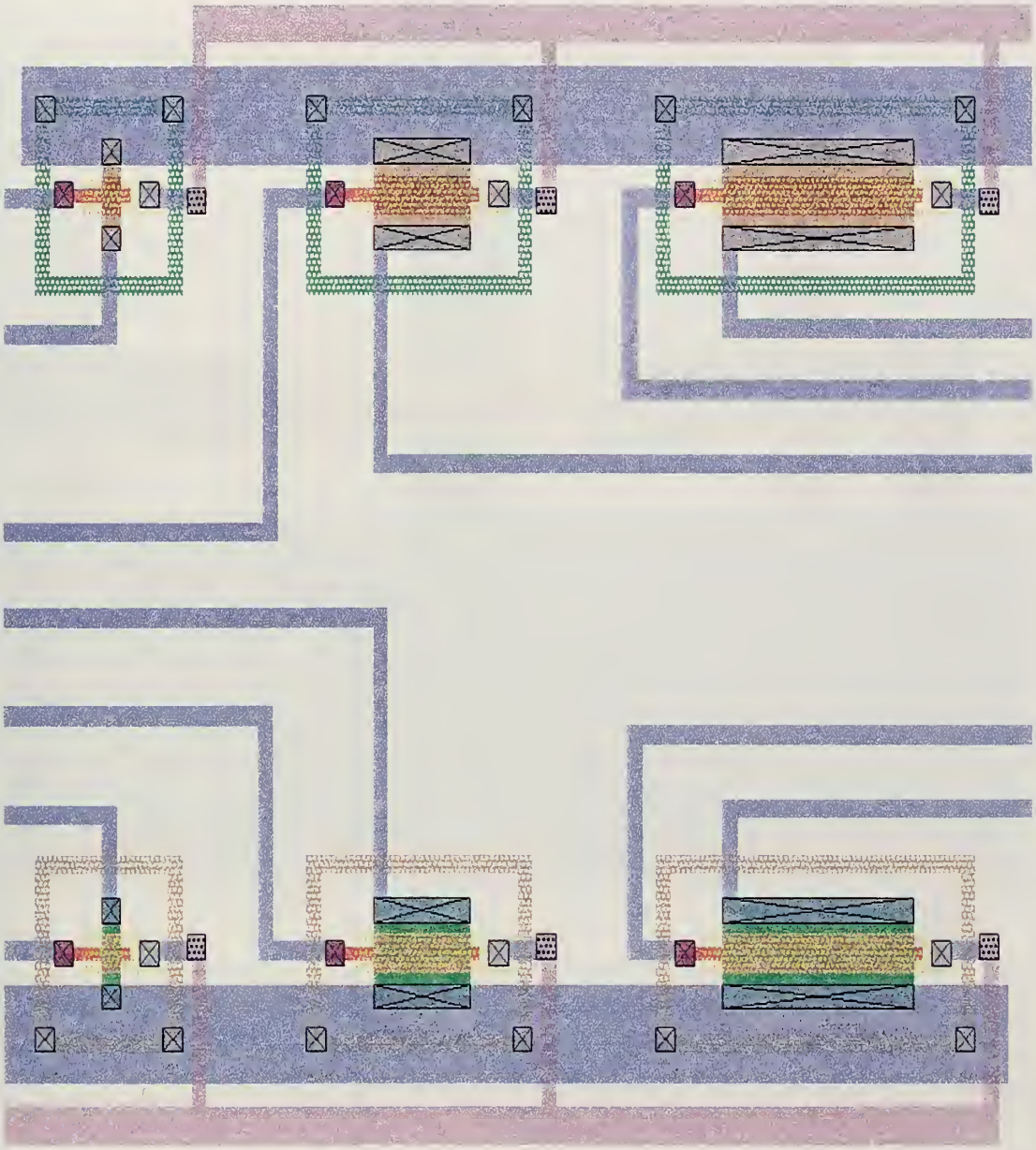


Figure B.31. Chip Two Structure Two.

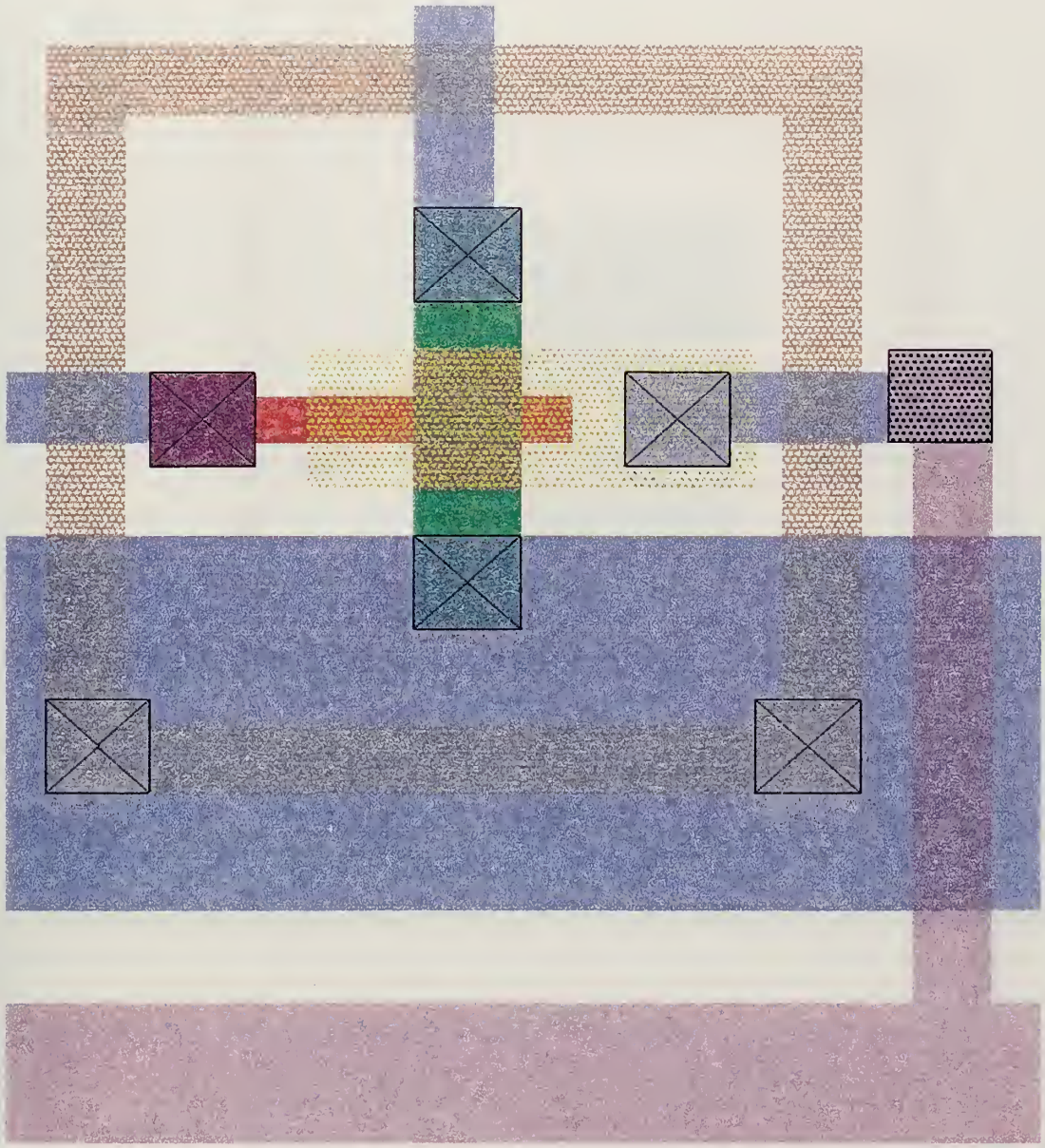


Figure B.32. Device 2N12.

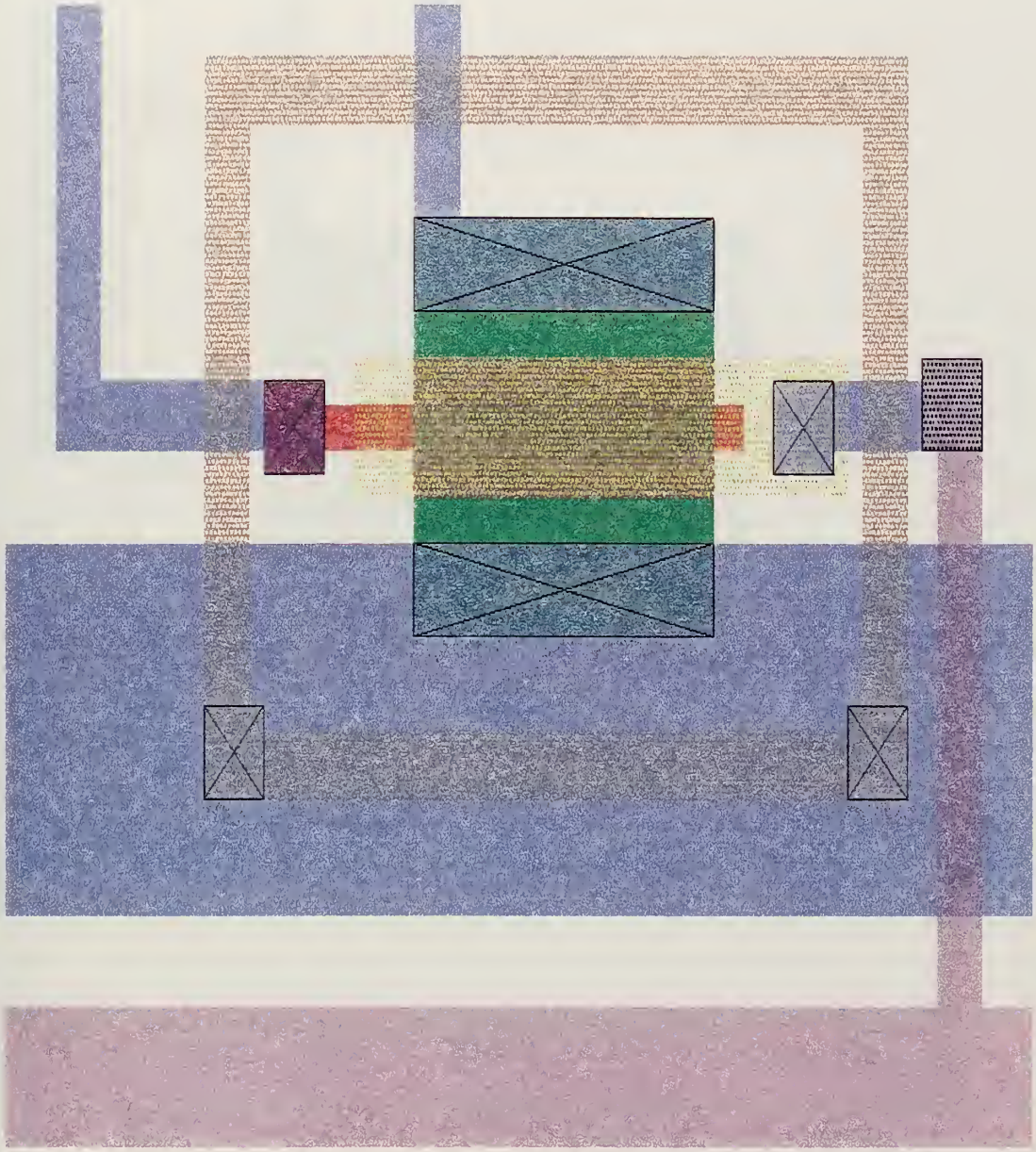


Figure B.33. Device 2N22.

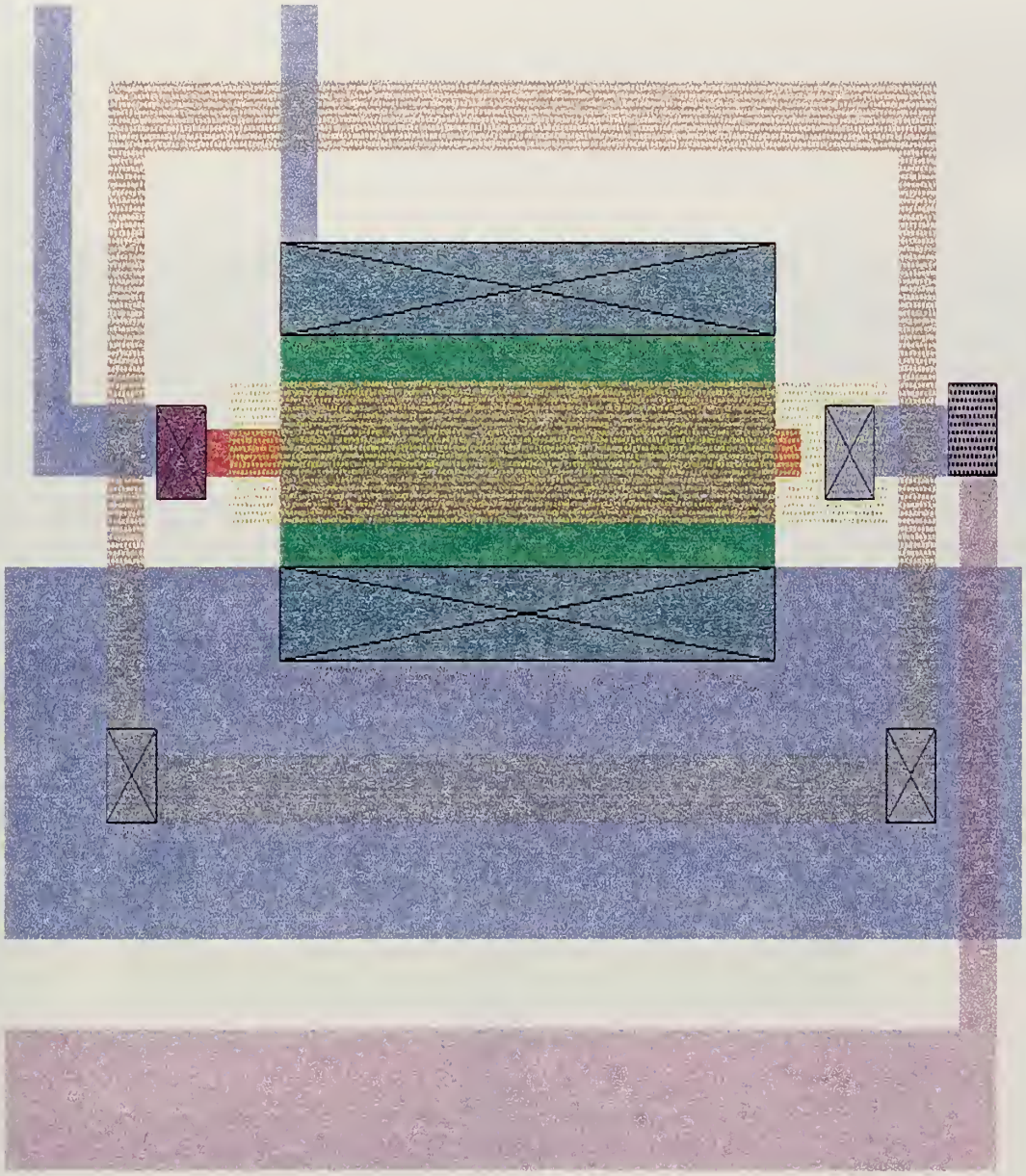


Figure B.34. Device 2N32.

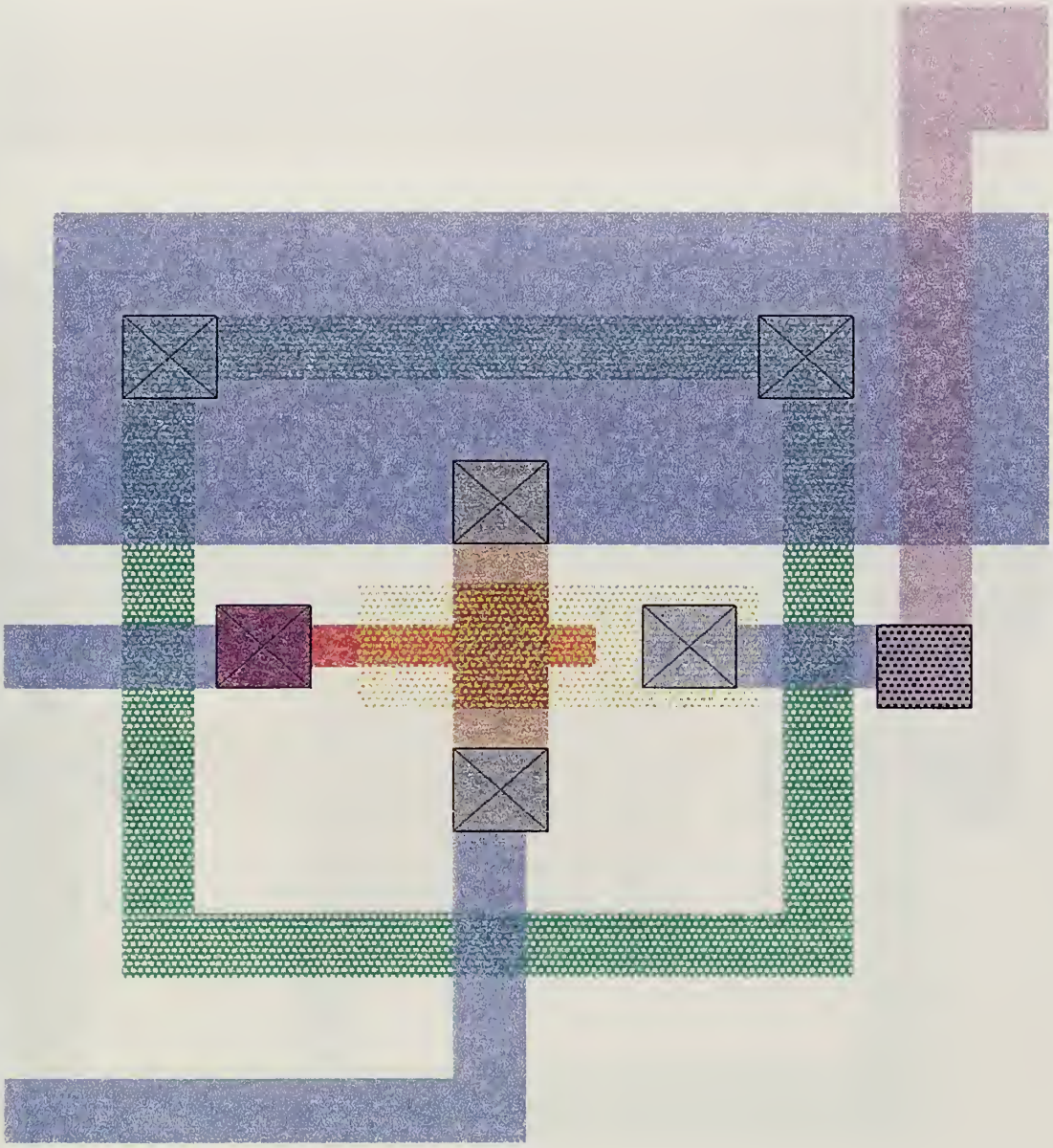


Figure B.35. Device 2P12.

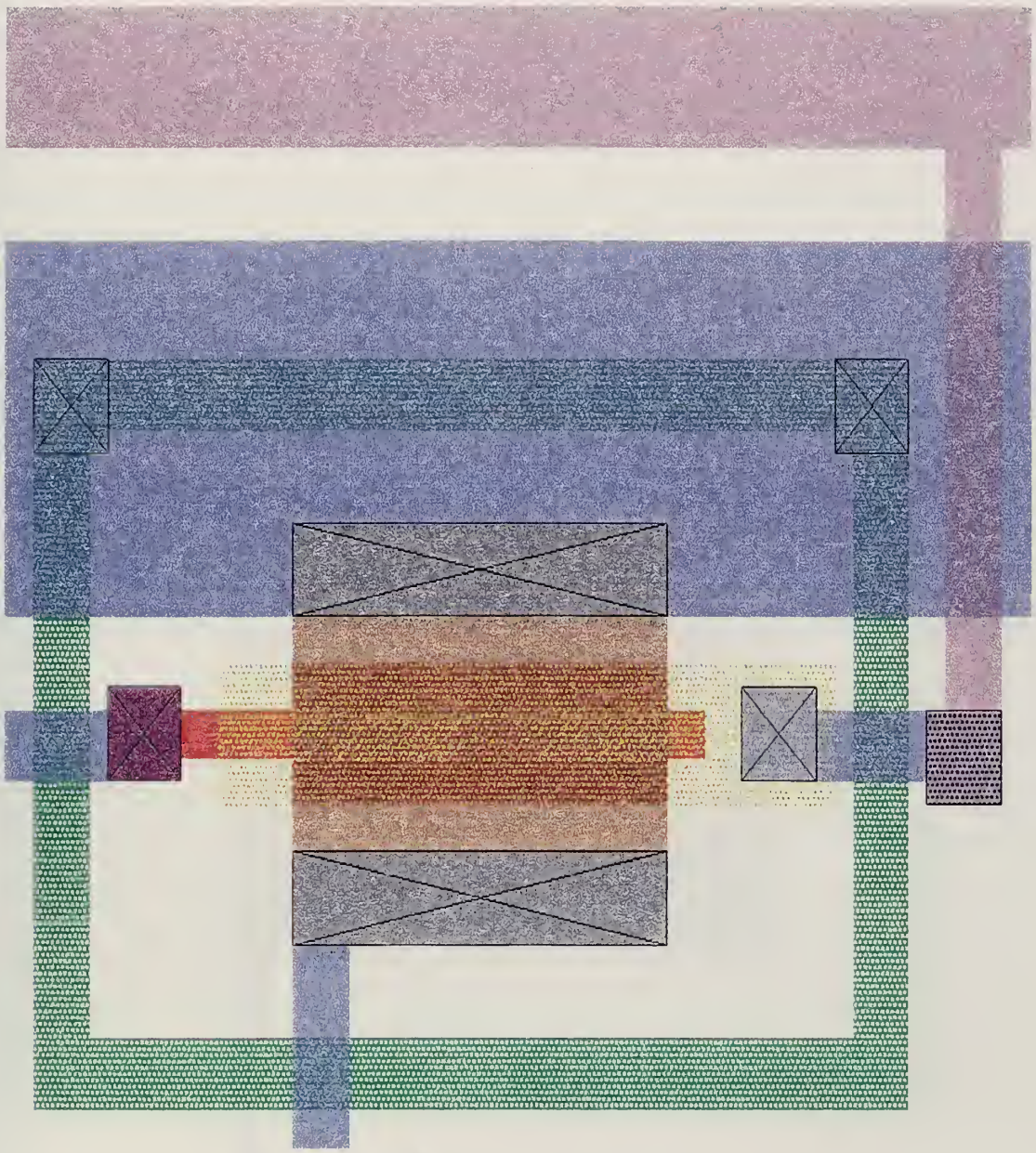


Figure B.36. Device 2P22.

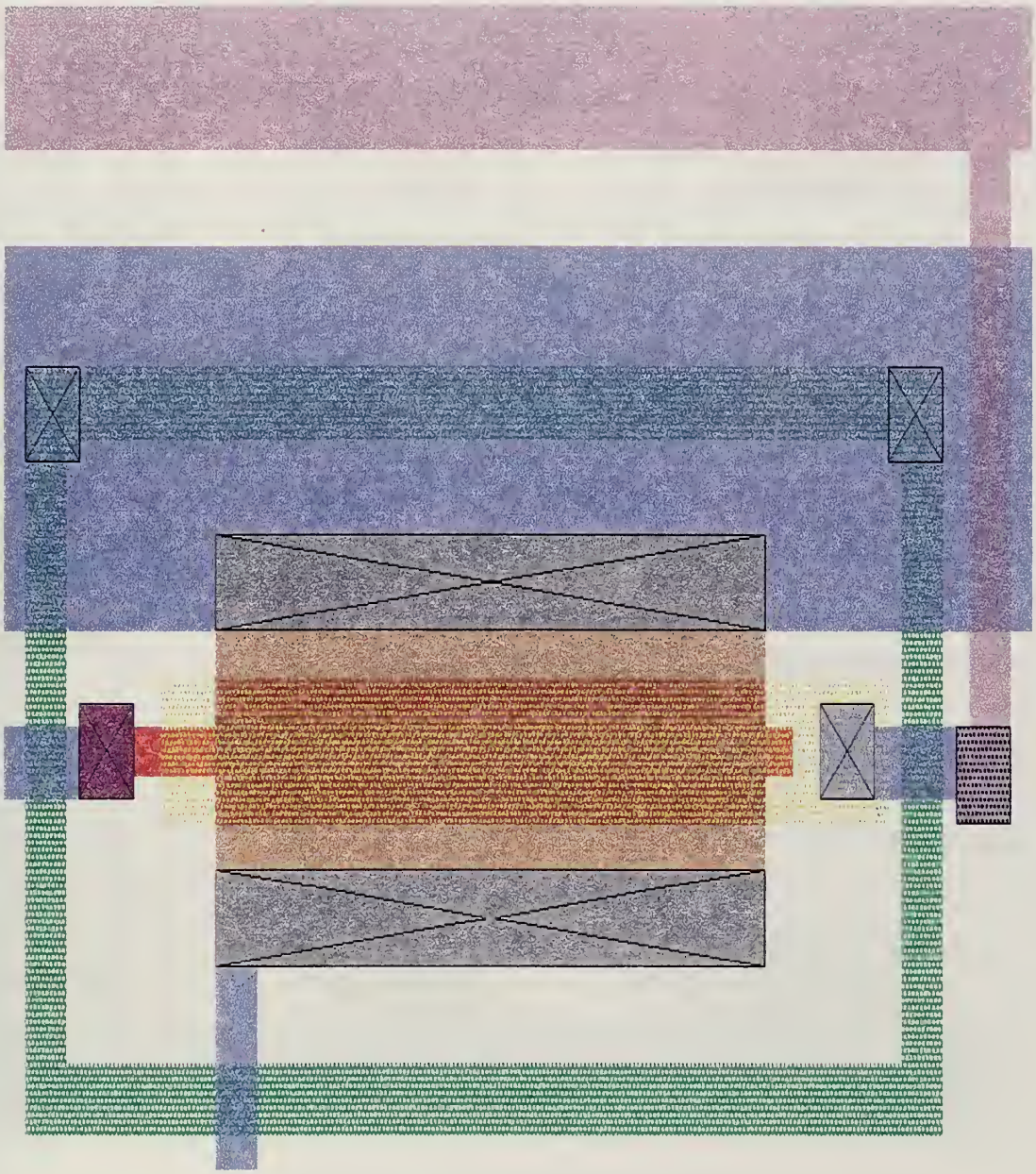


Figure B.37. Device 2P32.

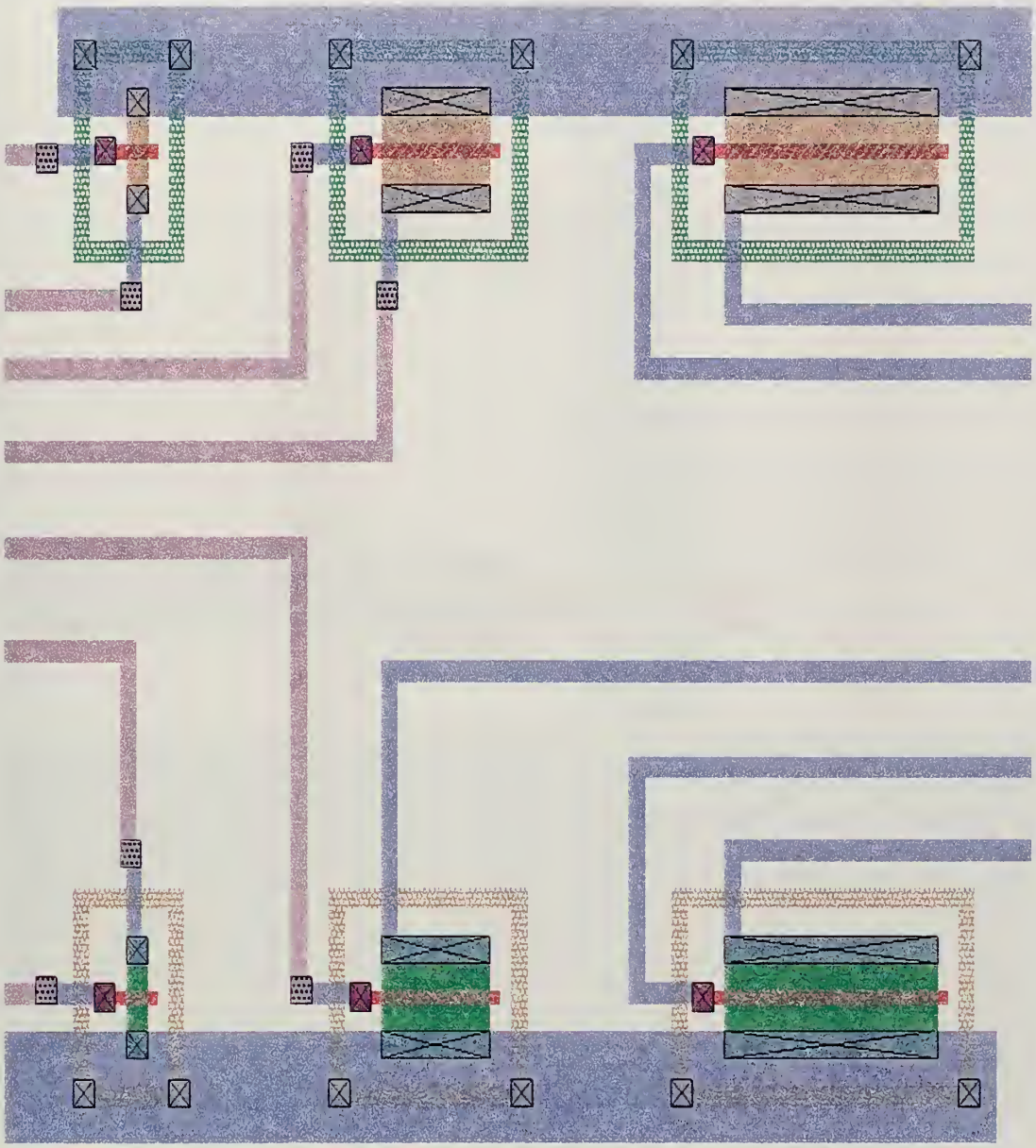


Figure B.38. Chip Two Structure Three.

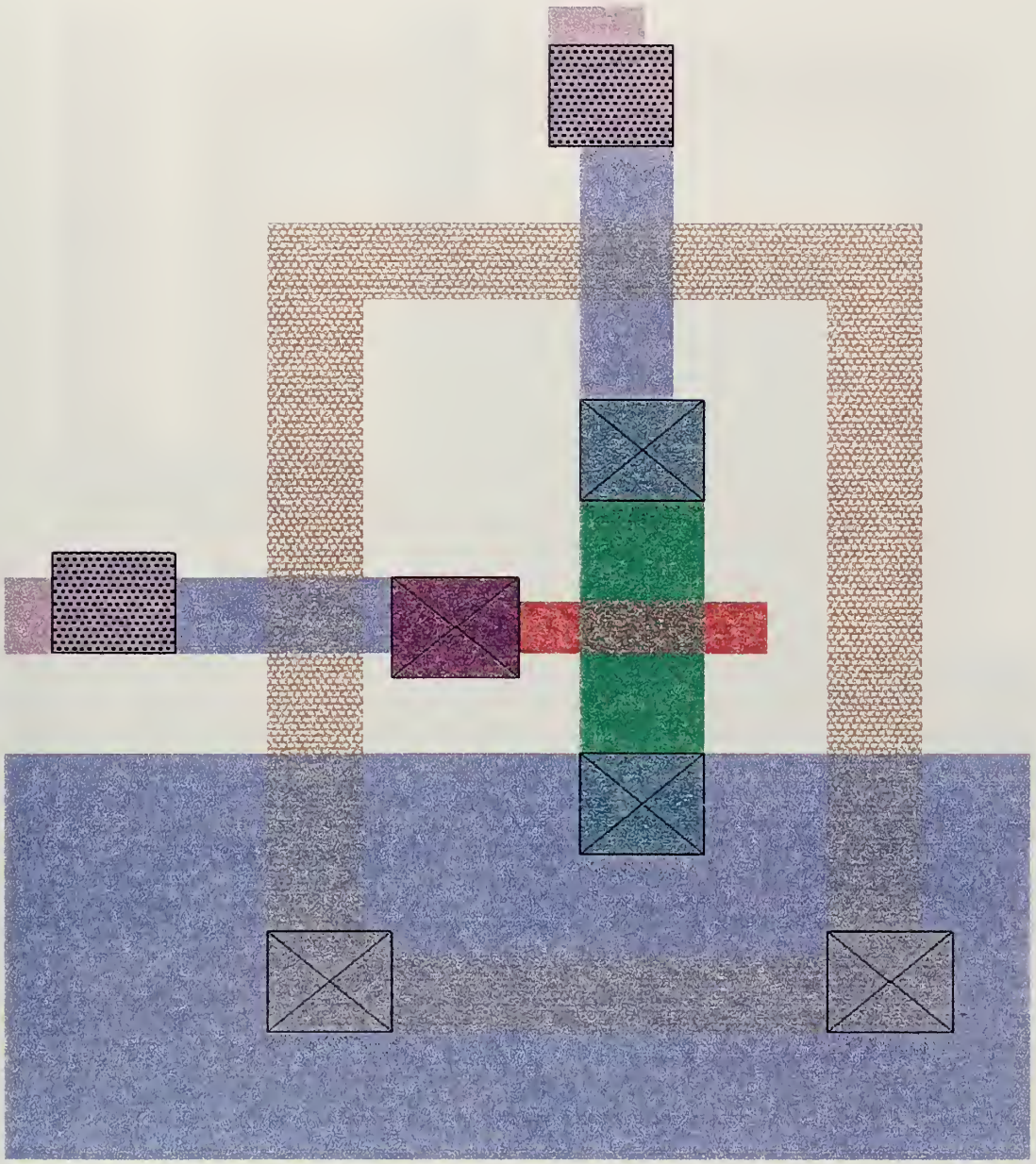


Figure B.39. Device 2N13.

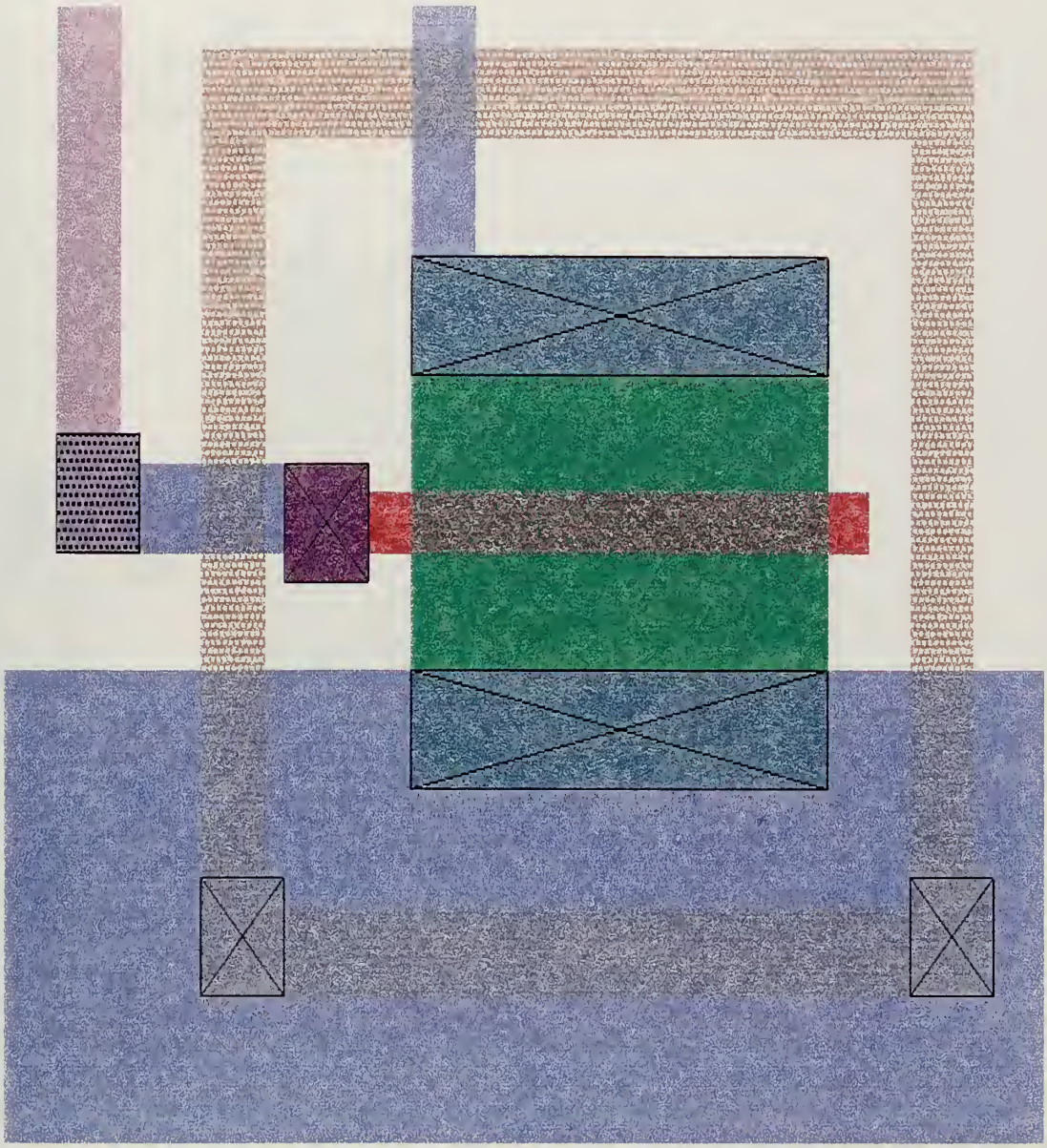


Figure B.40. Device 2N23.

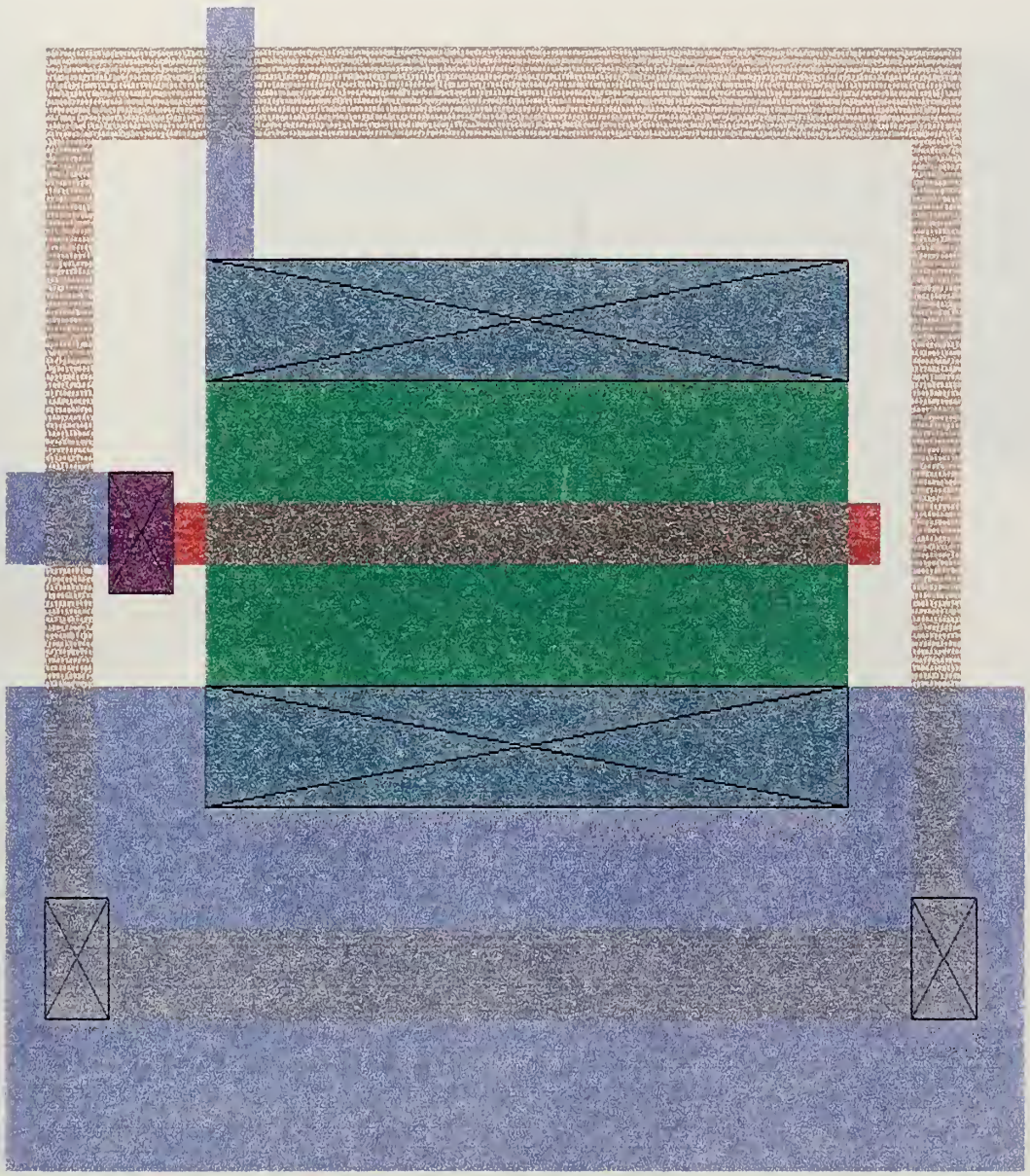


Figure B.41. Device 2N33.

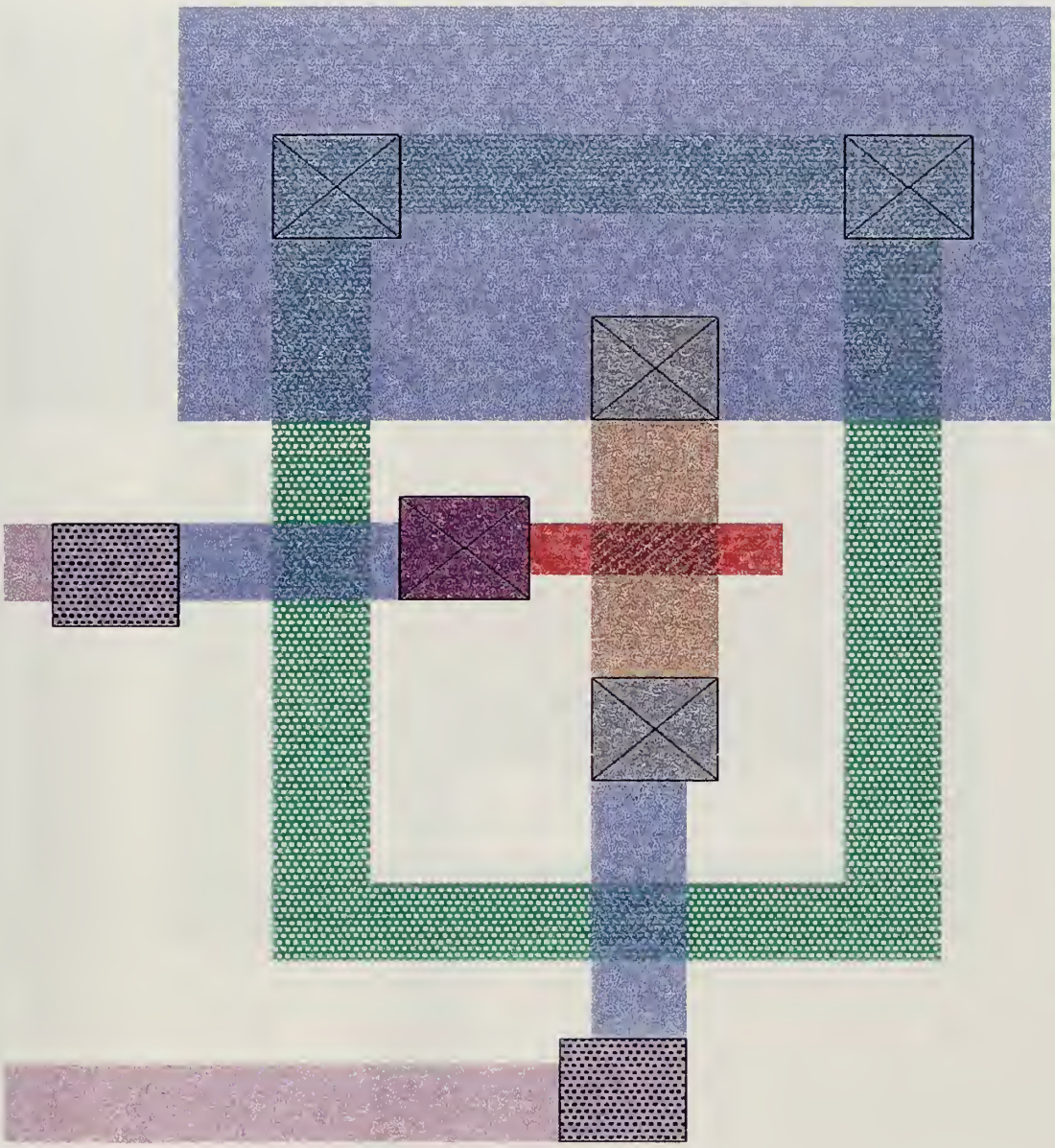


Figure B.42. Device 2P13.

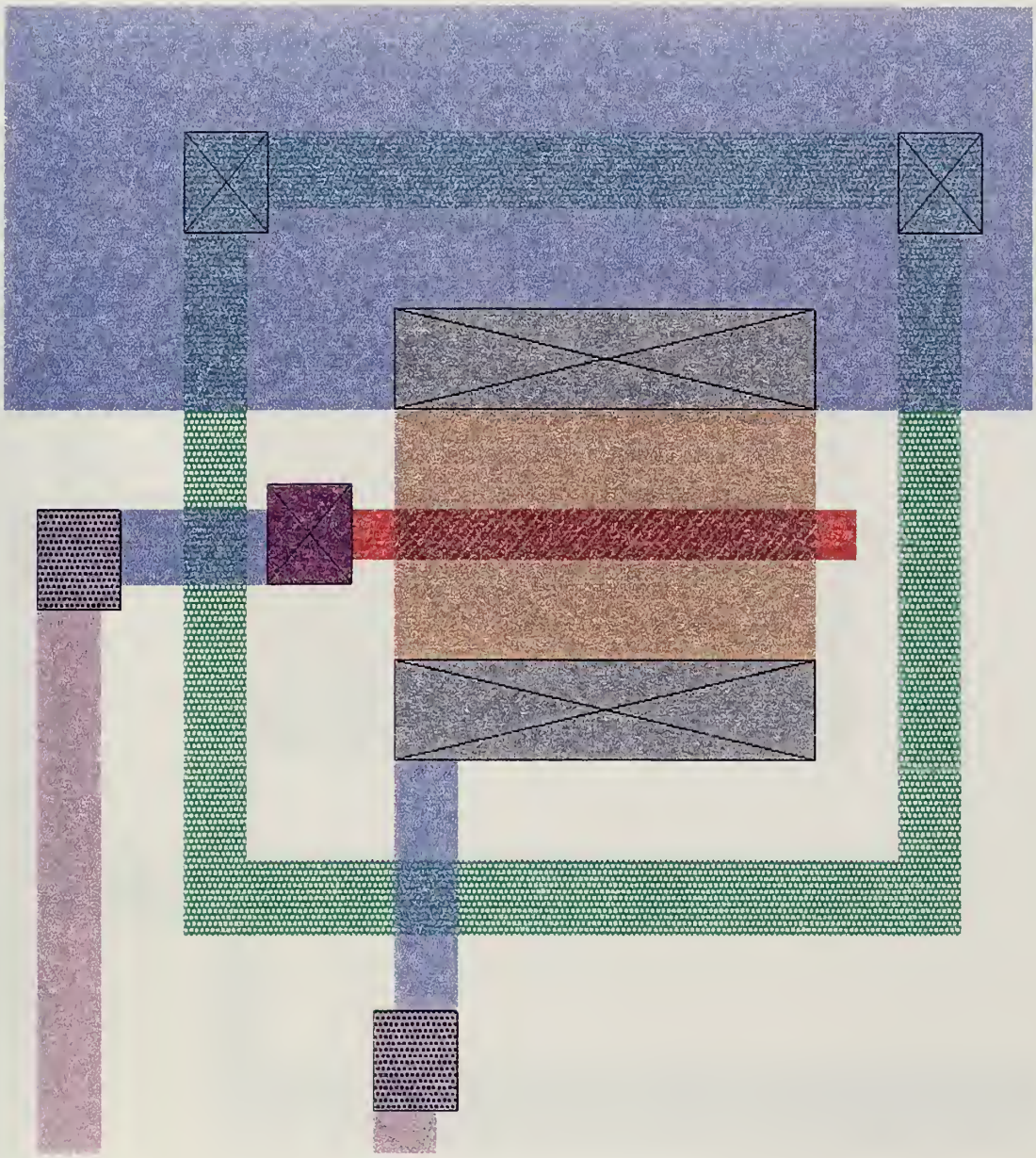


Figure B.43. Device 2P23.

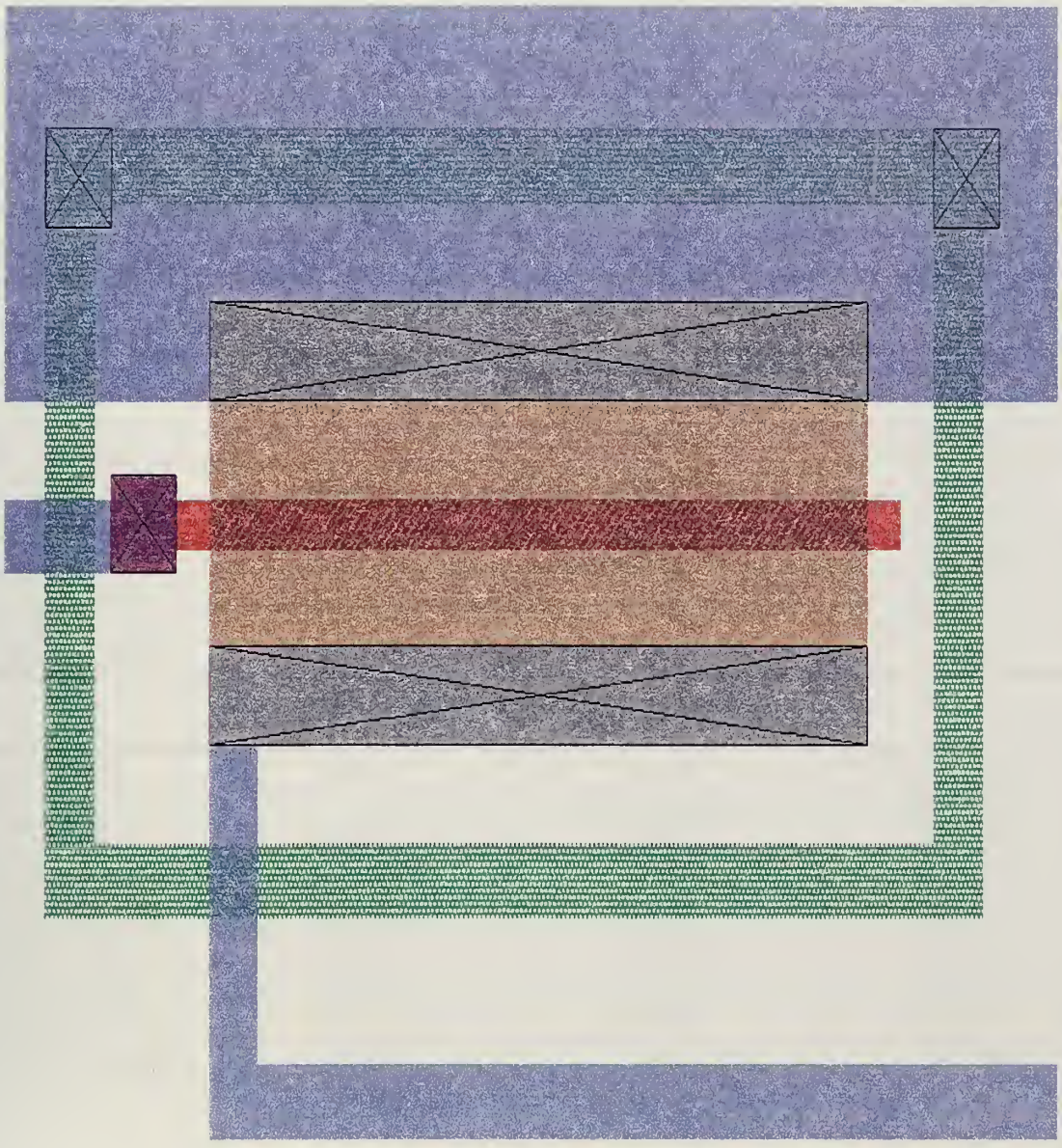


Figure B.44. Device 2P33.

APPENDIX C. TESTING RESULTS

This Appendix contains the plots and tables display the results obtained from the testing of chip one.

1N21	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$88.7x10^{-6}$	0.7605	3.25 pA
10 krad (Si)	$87.9x10^{-6}$	0.6723	18.05 pA
20 krad (Si)	$75.2x10^{-6}$	0.6674	52.83 nA
40 krad (Si)	$38.0x10^{-6}$	1.0091	57.61 nA
Post delay	$28.8x10^{-6}$	1.5822	844.2 pA
80 krad (Si)	$27.7x10^{-6}$	1.0654	5.098 nA
160 krad (Si)	$27.7x10^{-6}$	-0.7635	30.2 μA

Table C.1. Data Summary for Device 1N21.

1N31	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$165x10^{-6}$	0.7199	2.850 pA
10 krad (Si)	$164x10^{-6}$	0.6314	13.60 pA
20 krad (Si)	$161x10^{-6}$	0.5387	47.68 nA
40 krad (Si)	$159x10^{-6}$	0.3277	1.732 μA
Post delay	$157x10^{-6}$	0.4311	5.058 nA
80 krad (Si)	$151x10^{-6}$	0.2746	10.73 nA
160 krad (Si)	$133x10^{-6}$	NA	71.7 mA

Table C.2. Data Summary for Device 1N31.

1N22	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$64.8x10^{-6}$	0.7985	13.50 pA
10 krad (Si)	$64.6x10^{-6}$	0.7055	18.15 pA
20 krad (Si)	$61.1x10^{-6}$	0.6190	22.08 nA
40 krad (Si)	$60.1x10^{-6}$	0.4026	1.974 μA
Post delay	$58.8x10^{-6}$	0.5157	6.882 nA
80 krad(Si)	$55.7x10^{-6}$	0.3618	2.269 nA
160 krad (Si)	$51.3x10^{-6}$	NA	77.53 mA

Table C.3. Data Summary for Device 1N22.

1N32	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$125x10^{-6}$	0.7592	10.50 pA
10 krad (Si)	$112x10^{-6}$	0.7400	14.55 pA
20 krad (Si)	$105x10^{-6}$	0.6678	47.6 pA
40 krad (Si)	$161x10^{-6}$	0.4864	912.3 pA
Post delay	$26.3x10^{-6}$	0.5366	303.3 pA
80 krad (Si)	$96.2x10^{-6}$	0.3893	4.390 nA
160 krad (Si)	$91.8x10^{-6}$	-0.2773	24.48 μA

Table C.4. Data Summary for Device 1N32.

1N23	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$75.6x10^{-6}$	0.7694	3.45 pA
10 krad (Si)	$63.0x10^{-6}$	-0.8988	261.6 μA
20 krad (Si)	$60.3x10^{-6}$	-0.8916	244.4 μA
40 krad (Si)	$59.8x10^{-6}$	-1.0019	285.3 μA
Post delay	$56.7x10^{-6}$	-0.6155	109.1 μA
80 krad (Si)	$55.9x10^{-6}$	-0.5097	78.83 μA
160 krad (Si)	$55.5x10^{-6}$	-1.0377	269.9 μA

Table C.5. Data Summary for Device 1N23.

1N33	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$151x10^{-6}$	0.7099	8.300 pA
10 krad (Si)	$129x10^{-6}$	0.6745	18.05 pA
20 krad (Si)	$129x10^{-6}$	0.5741	6.759 nA
40 krad (Si)	$126x10^{-6}$	0.3615	1.164 μA
Post delay	$124x10^{-6}$	0.4522	3.849 nA
80 krad (Si)	$120x10^{-6}$	0.2882	12.76 nA
160 krad (Si)	$118x10^{-6}$	-0.3585	58.27 μA

Table C.6. Data Summary for Device 1N33.

1P21	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$38.6x10^{-6}$	-0.9575	-4.65 pA
10 krad (Si)	$36.6x10^{-6}$	-1.0646	-3.85 pA
20 krad (Si)	$35.4x10^{-6}$	-1.1729	-4.600 pA
40 krad (Si)	$33.8x10^{-6}$	-1.3815	-4.800 pA
Post delay	$33.5x10^{-6}$	-1.4626	-4.150 pA
80 krad (Si)	$33.0x10^{-6}$	-1.4626	-4.150 pA
160 krad (Si)	Burned	Out	

Table C.7. Data Summary for Device 1P21.

1P31	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$72.7x10^{-6}$	-0.9153	-8.800 pA
10 krad (Si)	$68.9x10^{-6}$	-1.0256	-8.55 pA
20 krad (Si)	$67.0x10^{-6}$	-1.1316	-8.750 pA
40 krad (Si)	$63.6x10^{-6}$	-1.3385	-8.450 pA
Post delay	$62.7x10^{-6}$	-1.3360	-7.450 pA
80 krad (Si)	$62.9x10^{-6}$	-1.4106	-8.100 pA
160 krad (Si)	$48.1x10^{-6}$	-2.4843	-8.650 pA

Table C.8. Data Summary for Device 1P31.

1P22	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$26.0x10^{-6}$	-1.0114	-15.2 pA
10 krad (Si)	$24.7x10^{-6}$	-1.1309	-22.1 pA
20 krad (Si)	$24.1x10^{-6}$	-1.2481	-15.85 pA
40 krad (Si)	$22.8x10^{-6}$	-1.4772	-15.3 pA
Post delay	$22.0x10^{-6}$	-1.5099	-13.6 pA
80 krad (Si)	$22.0x10^{-6}$	-1.5820	-14.50 pA
160 krad (Si)	Burned	Out	

Table C.9. Data Summary for Device 1P22.

1P32	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$53.5x10^{-6}$	-0.9614	-10.25 pA
10 krad (Si)	$50.8x10^{-6}$	-1.0688	-14.65 pA
20 krad (Si)	$49.0x10^{-6}$	-1.1807	-10.55 pA
40 krad (Si)	$47.0x10^{-6}$	-1.3924	-10.35 pA
Post delay	$47.0x10^{-6}$	-1.3784	-9.300 pA
80 krad (Si)	$46.8x10^{-6}$	-1.4508	-11.20 pA
160 krad (Si)	$27.8x10^{-6}$	-2.5770	-12.00 pA

Table C.10. Data Summary for Device 1P32.

1P23	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$32.6x10^{-6}$	-0.9622	-4.850 pA
10 krad (Si)	$1.23x10^{6}$	-3.7485	-5.2 pA
20 krad (Si)	$1.33x10^{-6}$	-3.8910	-5.05 pA
40 krad (Si)	no maximum	-4.1545	-4.750 pA
Post delay	~$885x10^{-9}$	-4.1145	-4.750 pA
80 krad (Si)	$33.0x10^{-6}$	-1.4626	-4.150 pA
160 krad (Si)	~$941x10^{-9}$	-4.8250	-5.850 pA

Table C.11. Data Summary for Device 1P23.

1P33	G_M	V_T (V) (I_{DS} = 1 μA)	I_{DS} (V_G = 0, V_{DS} = 5V)
Pre-rad	$66.6x10^{-6}$	-0.9152	-3.950 pA
10 krad (Si)	$50.6x10^{-6}$	-2.7475	-5.15 pA
20 krad (Si)	$1.1x10^{-6}$	-2.8410	-4.200 pA
40 krad (Si)	$48.8x10^{-6}$	-3.0575	-4.050 pA
Post delay	~$930x10^{-9}$	-2.9885	-4.650 pA
80 krad (Si)	$45.9x10^{-6}$	-2.9250	-4.150 pA
160 krad (Si)	~$44.7x10^{-6}$	-3.6600	-6.900 pA

Table C.12. Data Summary for Device 1P33.

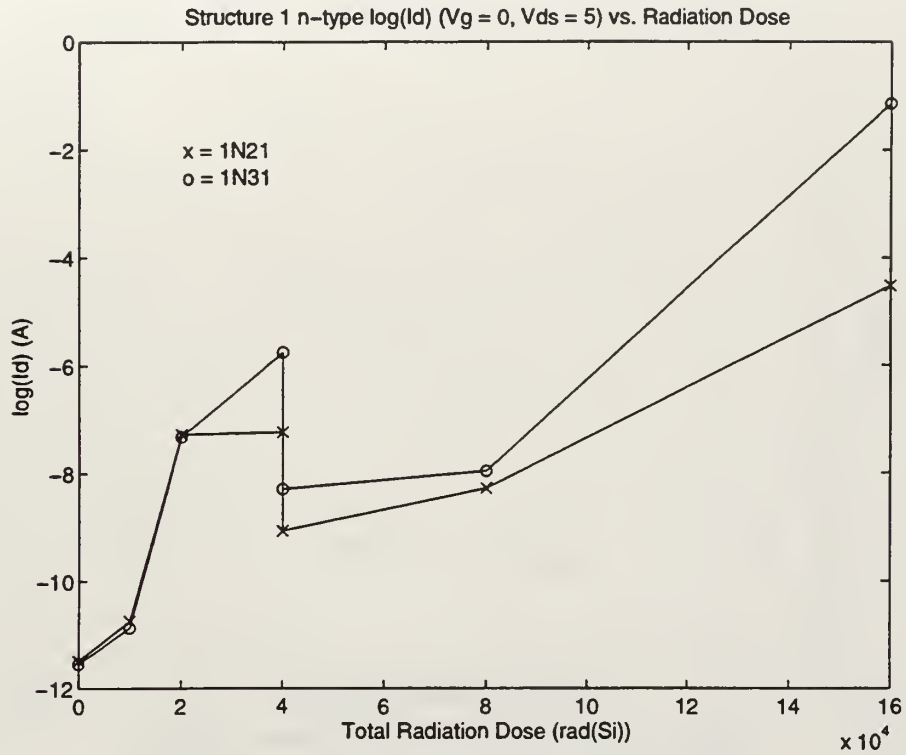


Figure C.1. Size Comparison for Structure 1 NFETs.

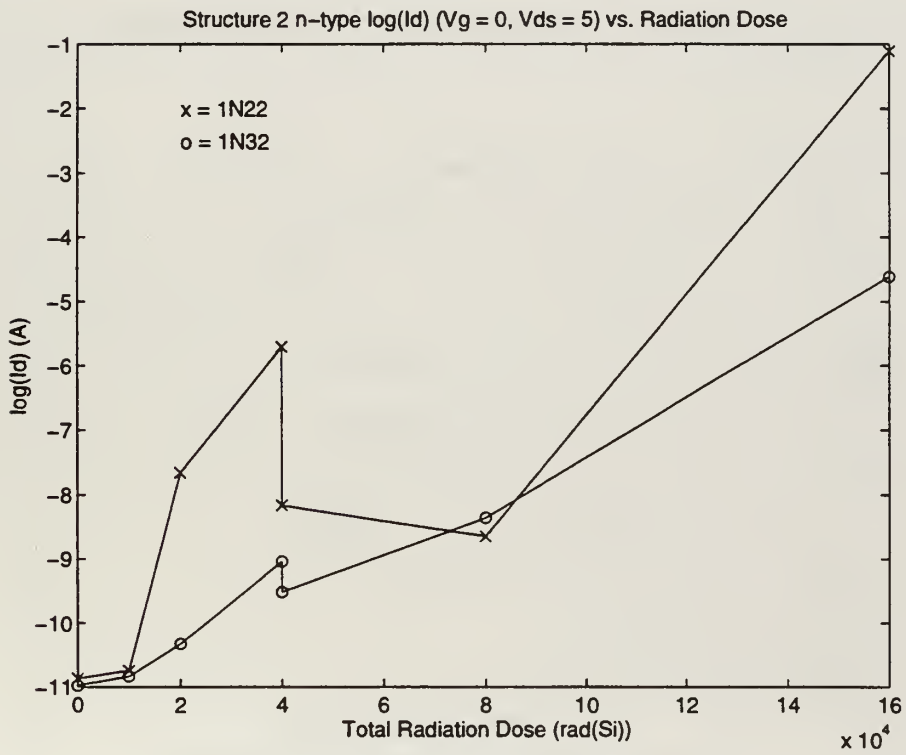


Figure C.2. Size Comparison for Structure 2 NFETs.

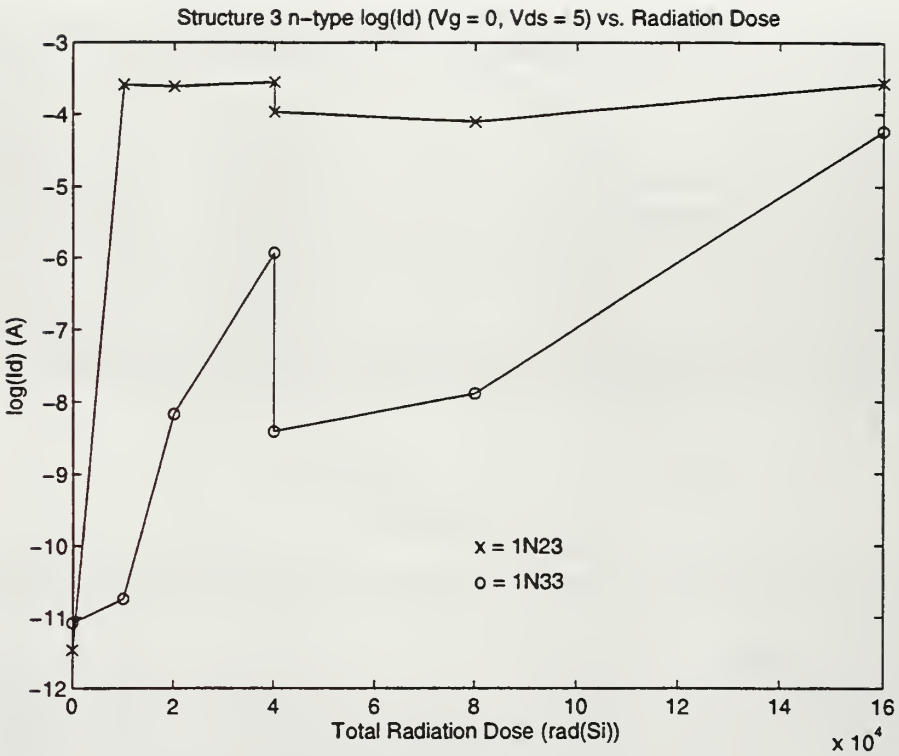


Figure C.3. Size Comparison for Structure 3 NFETs.

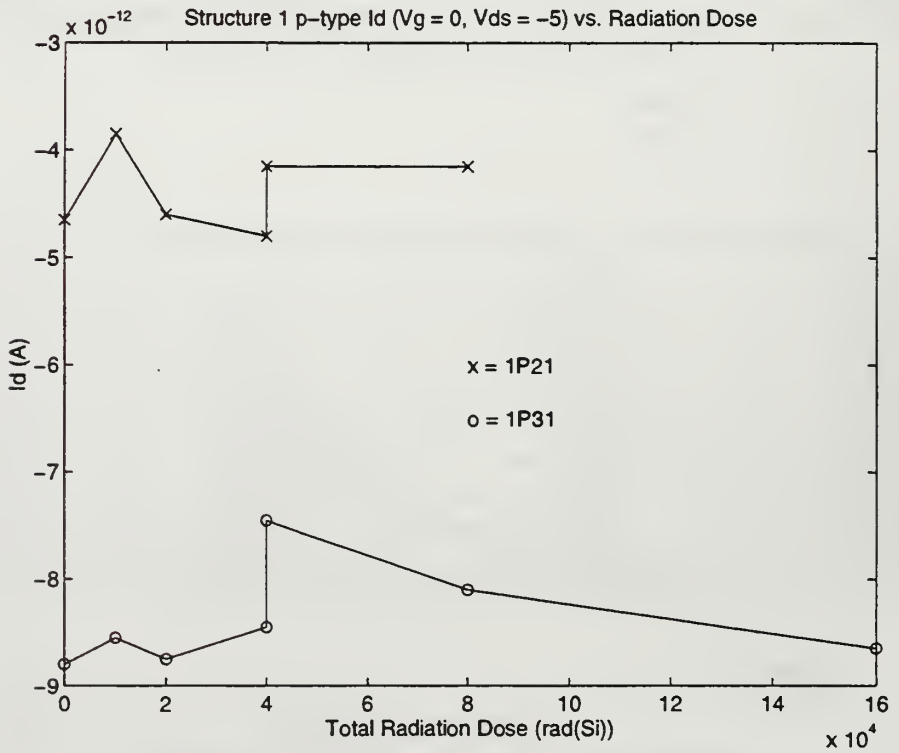


Figure C.4. Size Comparison for Structure 1 PFETs.

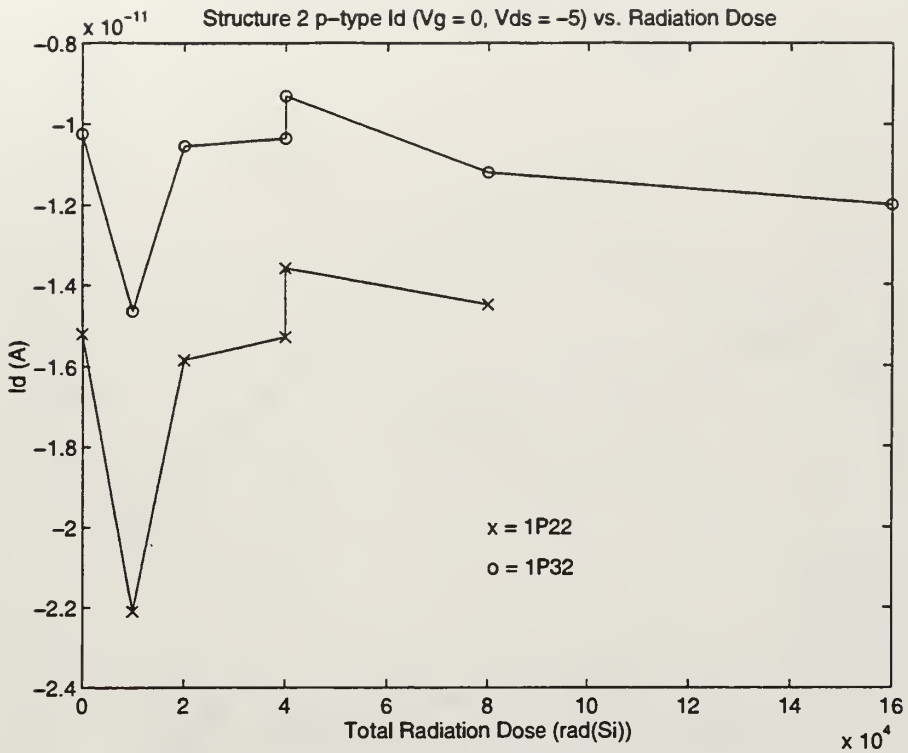


Figure C.5. Size Comparison for Structure 2 PFETs.

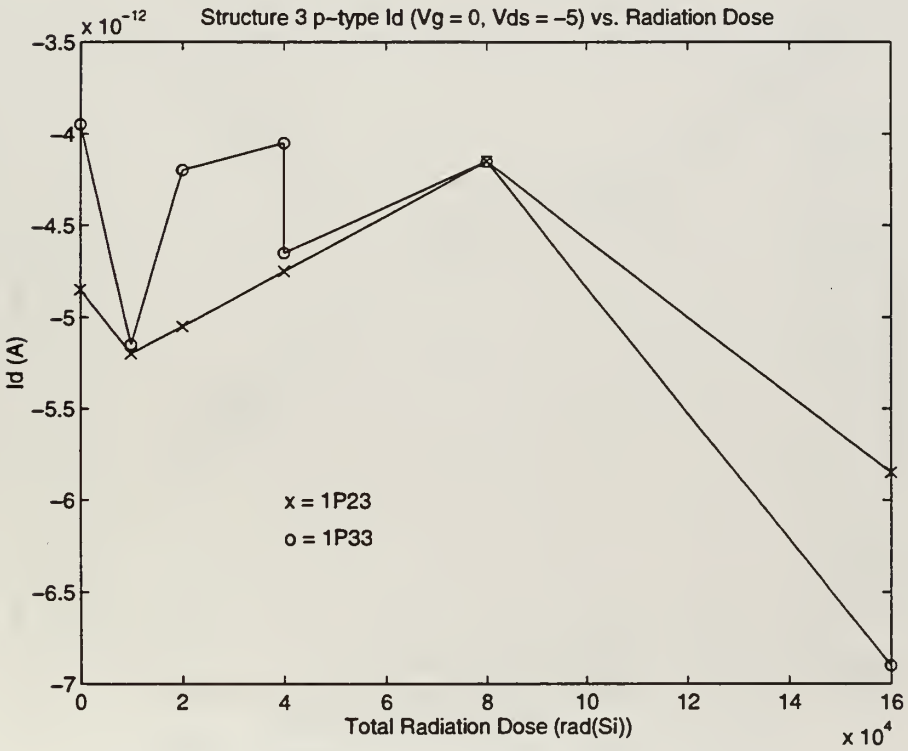


Figure C.6. Size Comparison for Structure 3 PFETs.

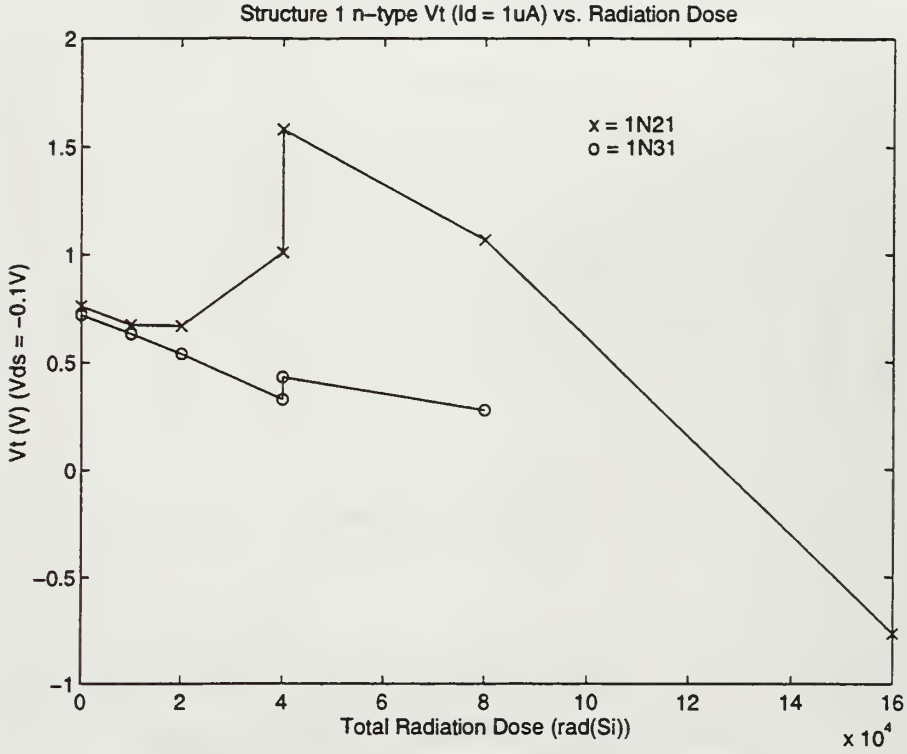


Figure C.7. Size Comparison for Structure 1 NFETs.

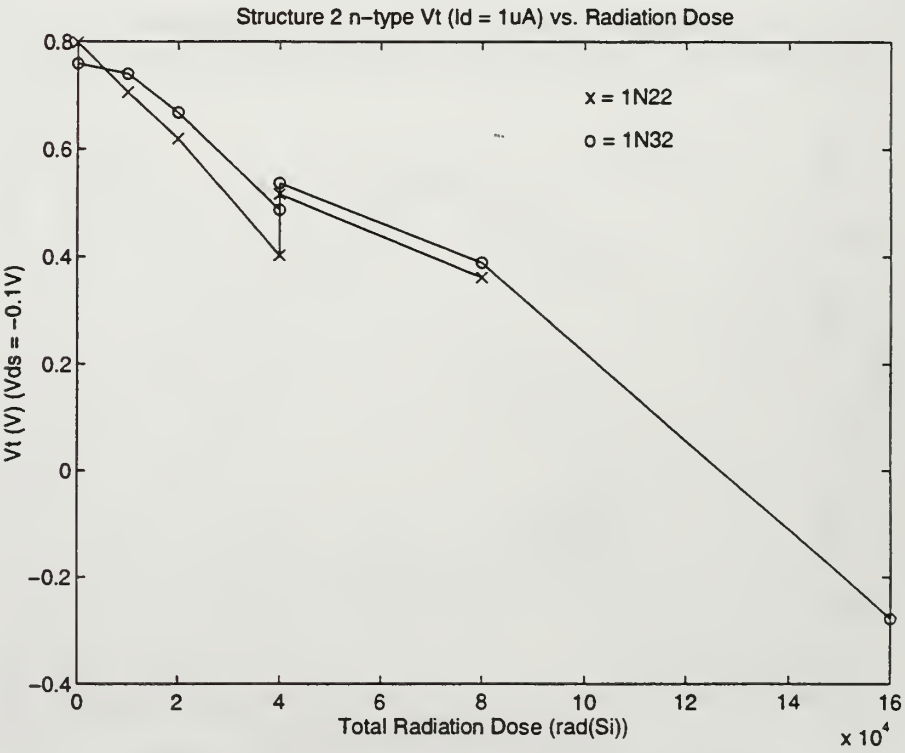


Figure C.8. Size Comparison for Structure 2 NFETs.

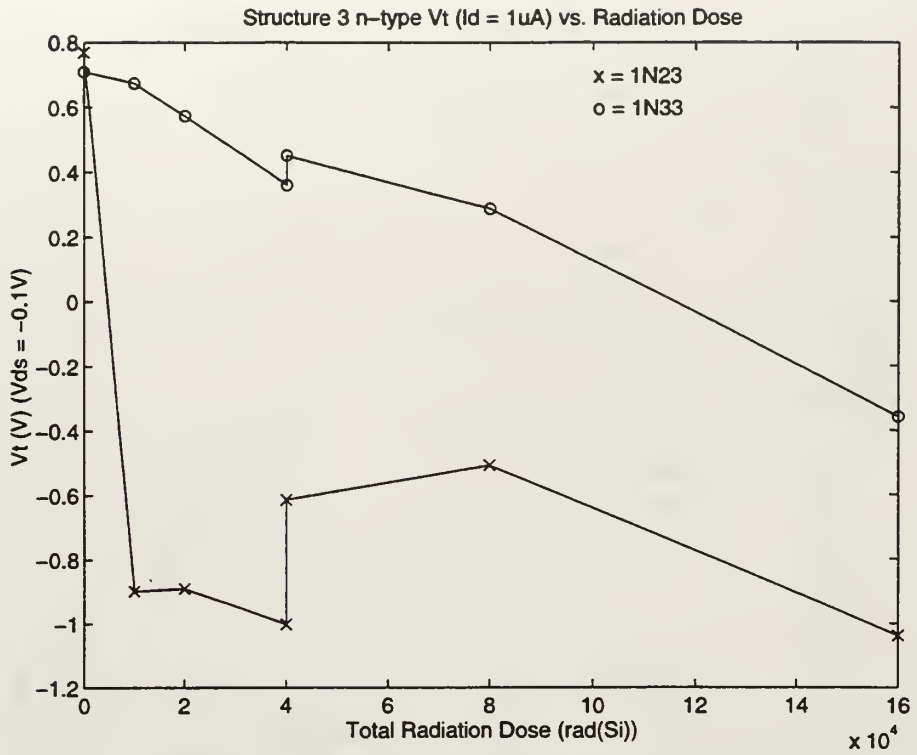


Figure C.9. Size Comparison for Structure 3 NFETs.

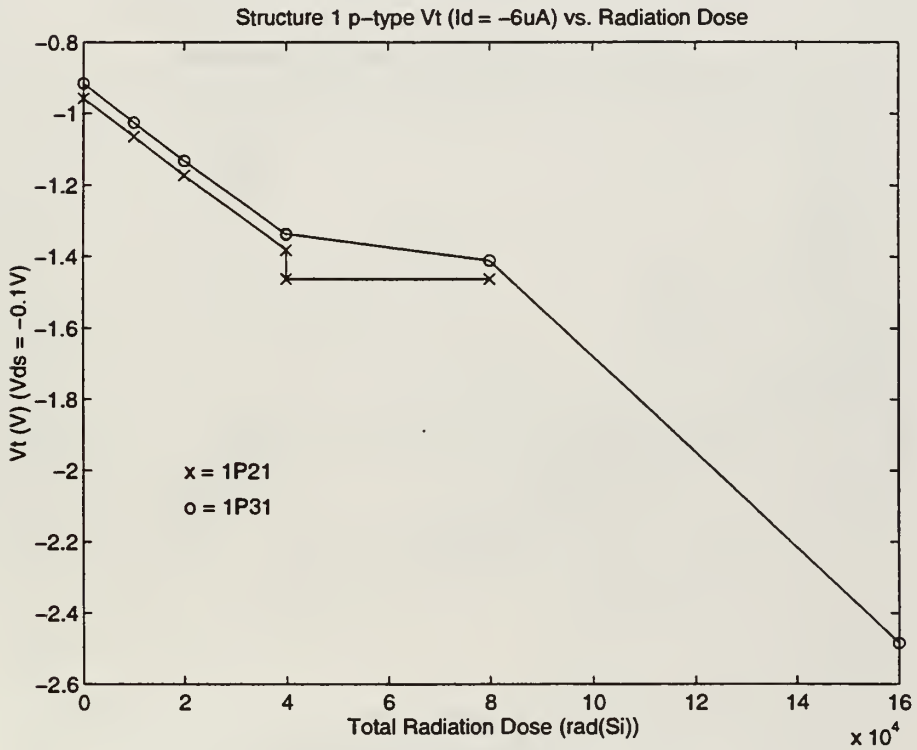


Figure C.10. Size Comparison for Structure 1 PFETs.

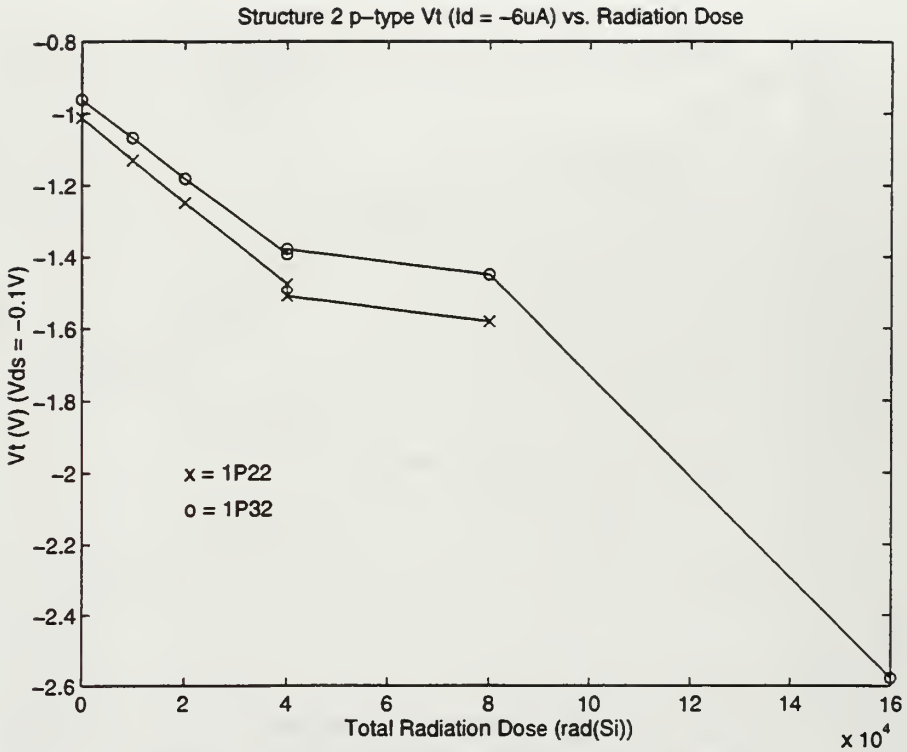


Figure C.11. Size Comparison for Structure 2 PFETs.

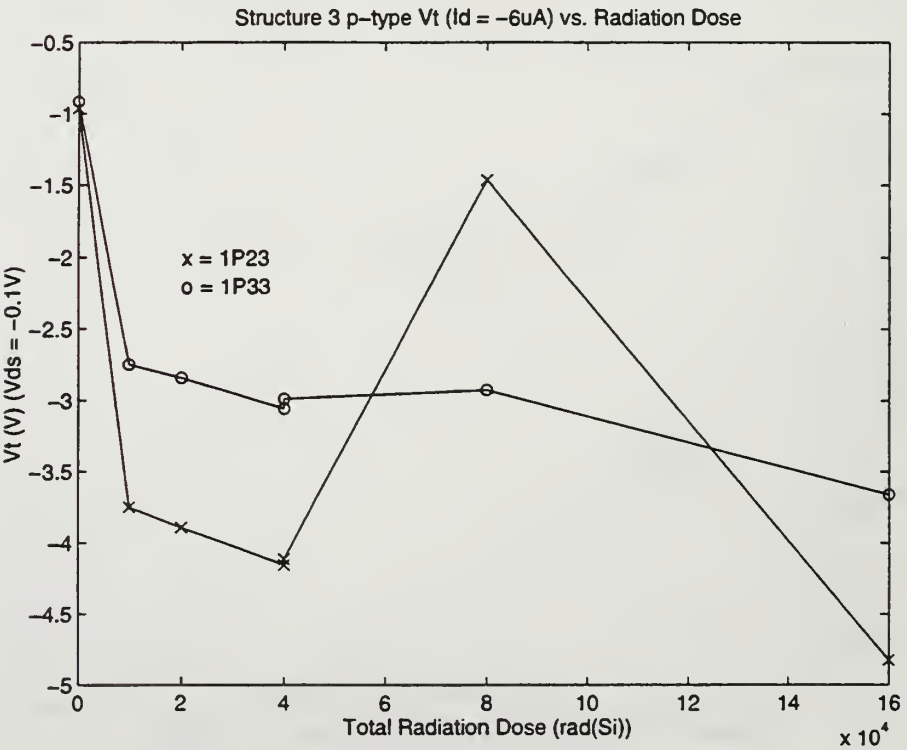


Figure C.12. Size Comparison for Structure 3 PFETs.

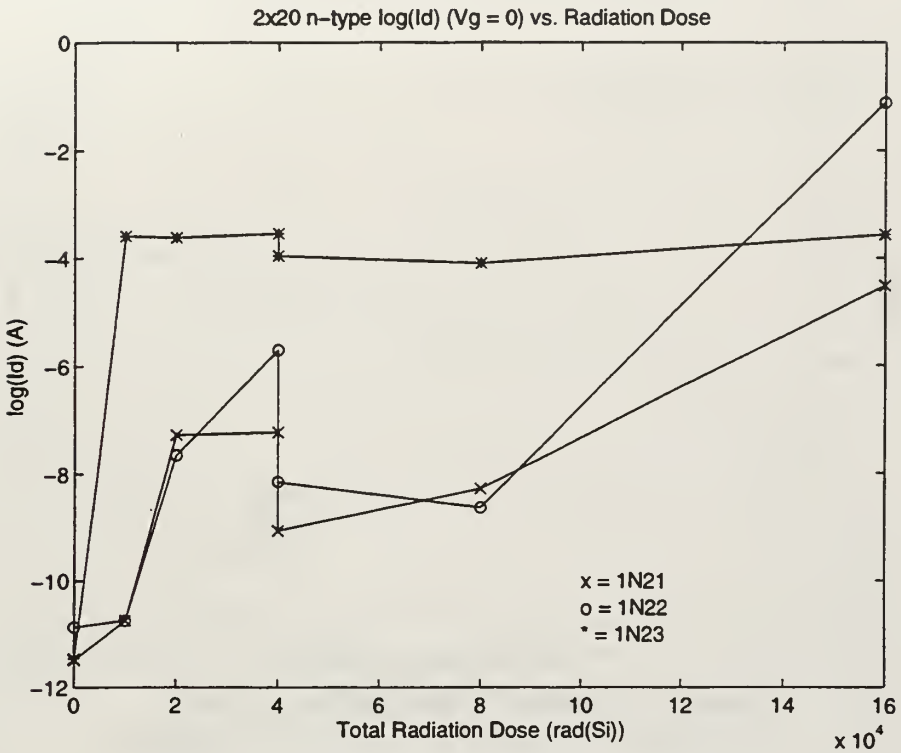


Figure C.13. Structure Comparison for 2x20 NFETs.

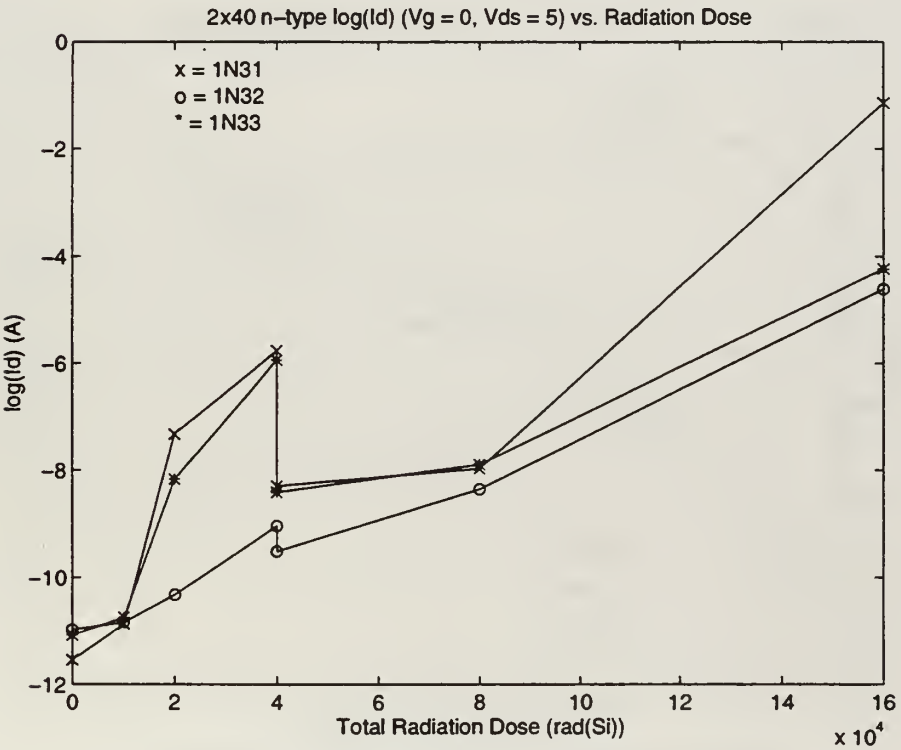


Figure C.14. Structure Comparison for 2x40 NFETs.

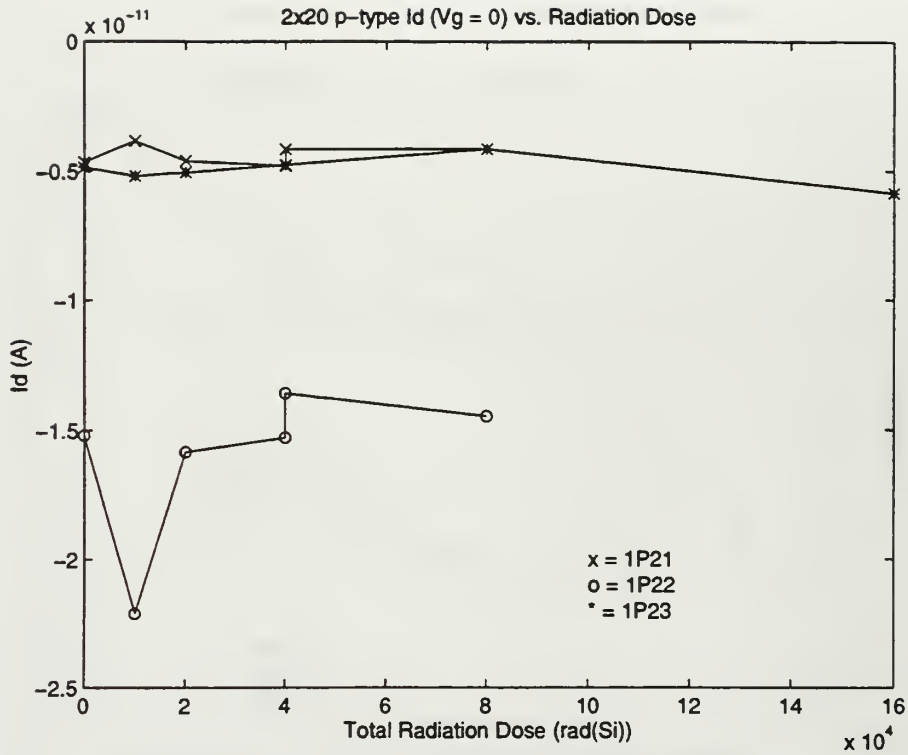


Figure C.15. Structure Comparison for 2x20 PFETs.

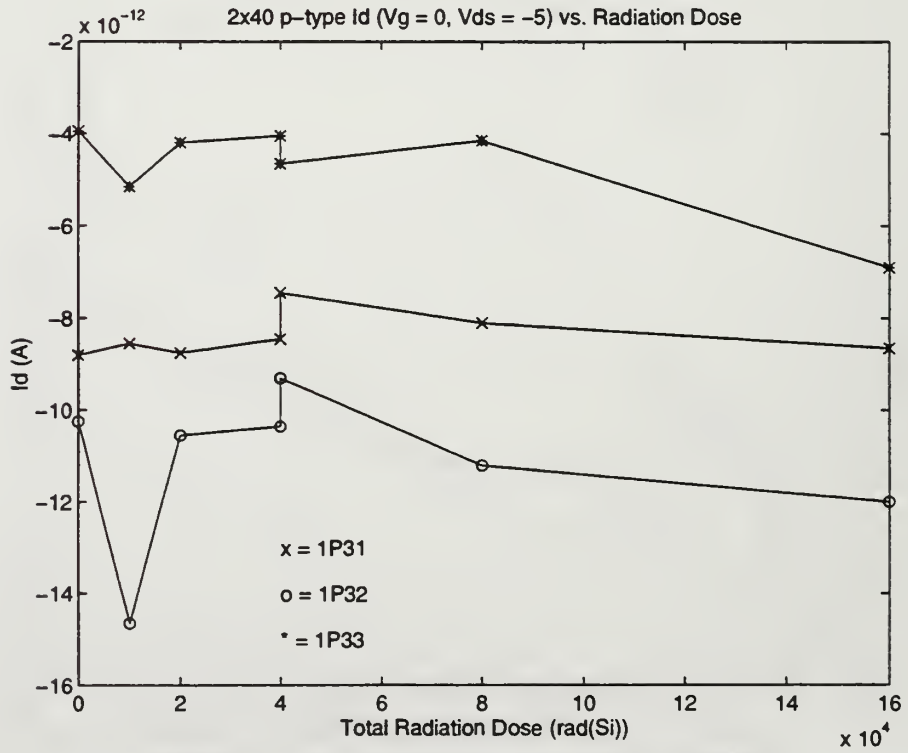


Figure C.16. Structure Comparison for 2x40 PFETs.

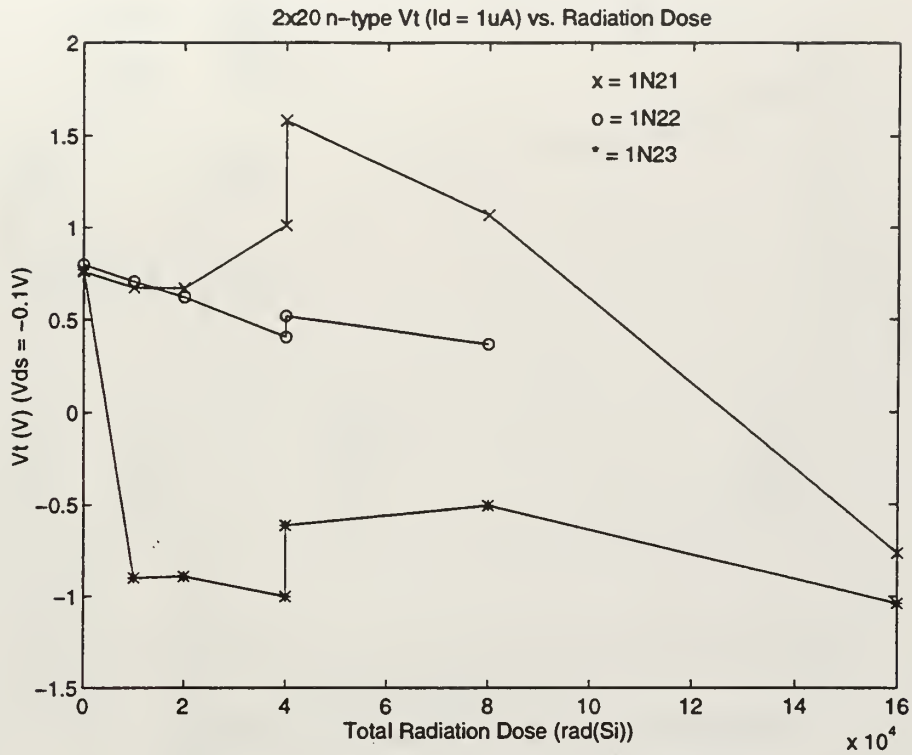


Figure C.17. Structure Comparison for 2x20 NFETs.

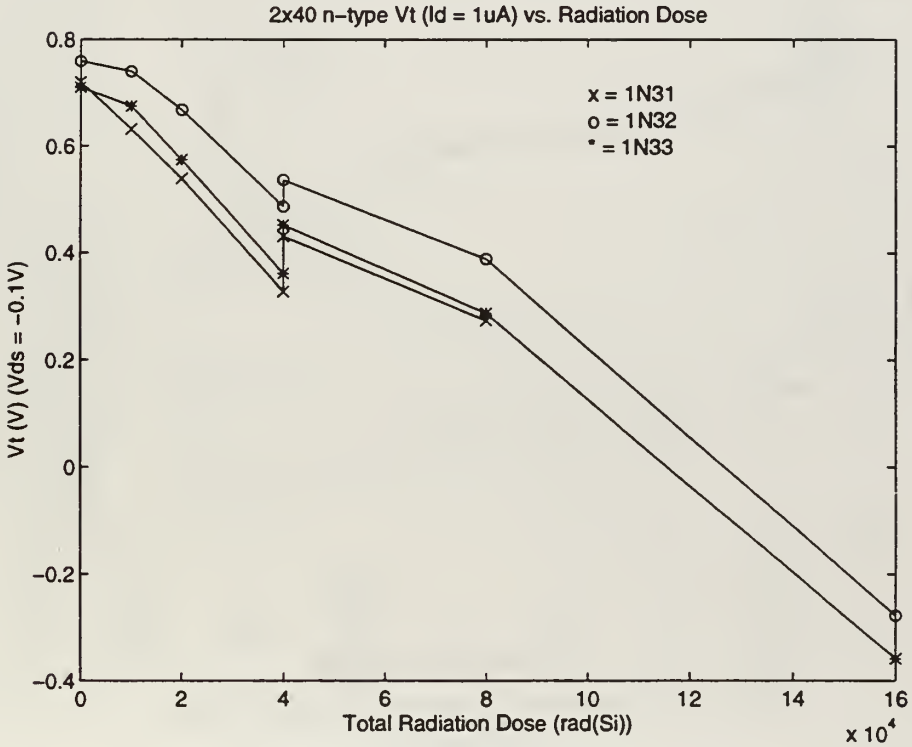


Figure C.18. Structure Comparison for 2x40 NFETs.

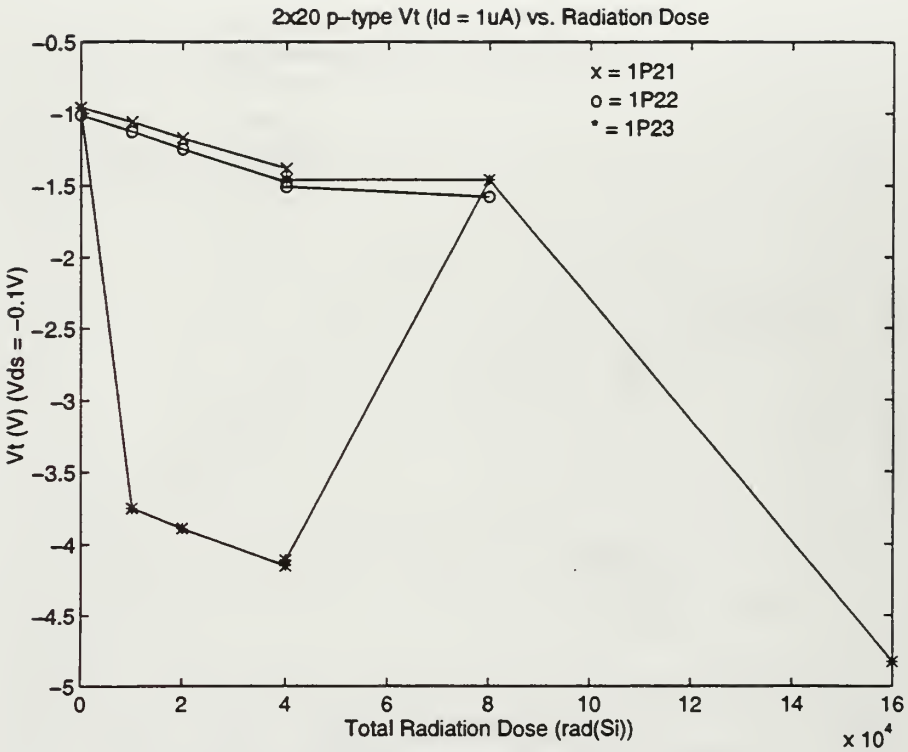


Figure C.19. Structure Comparison for 2x20 PFETs.

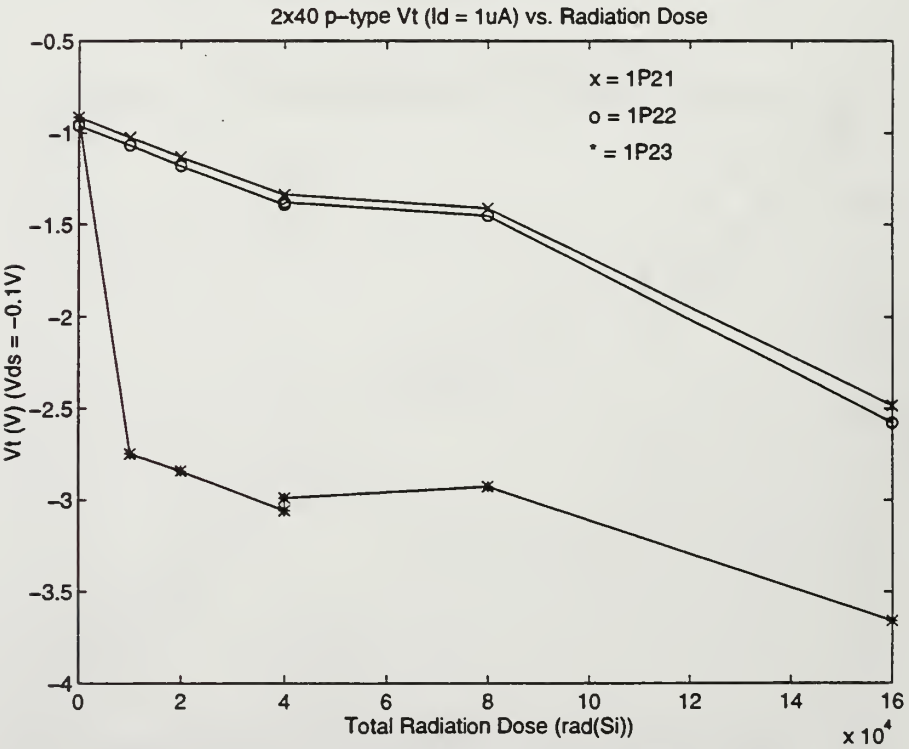


Figure C.20. Structure Comparison for 2x40 PFETs.

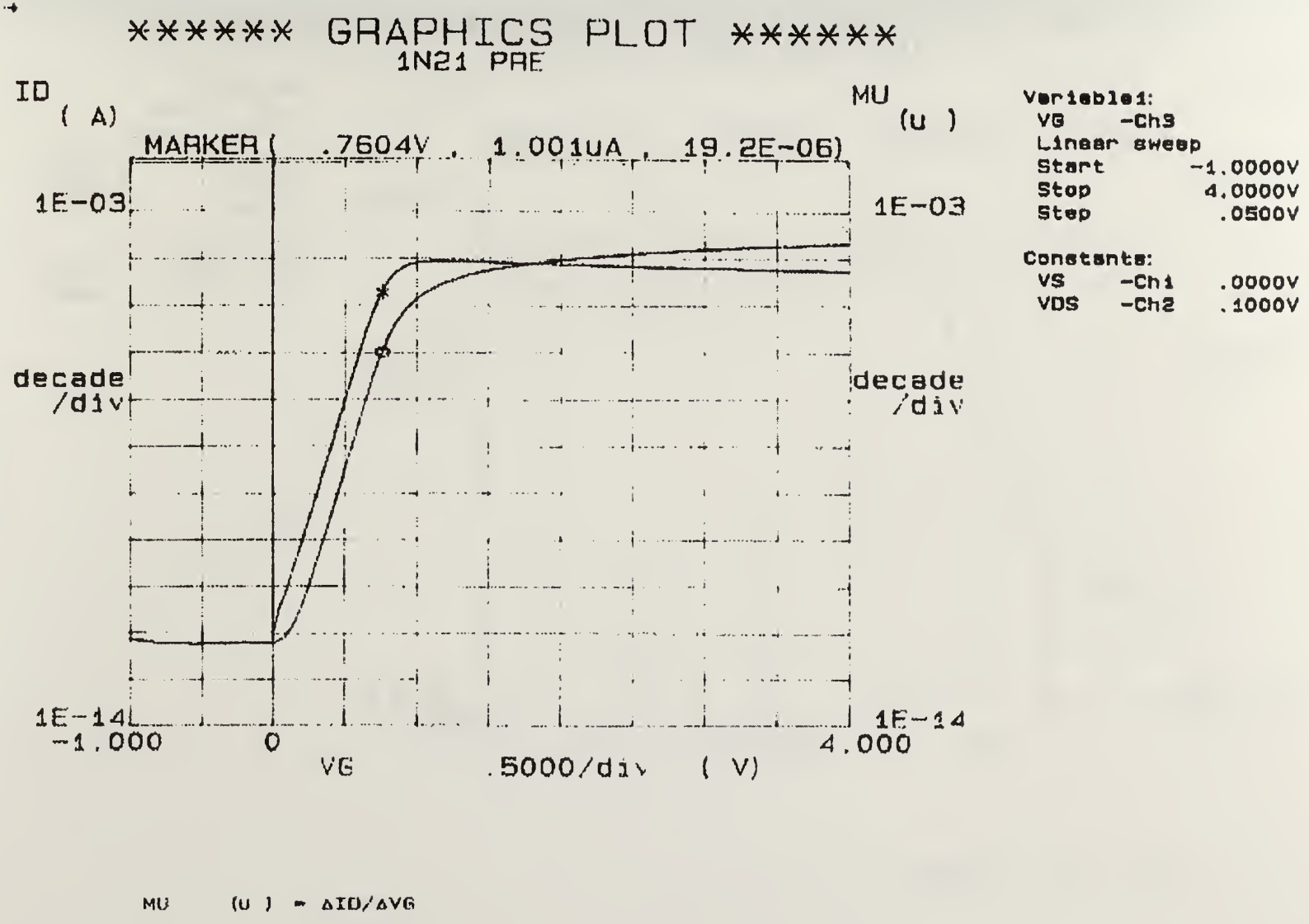

****** GRAPHICS PLOT ******
1N21 PRE
ID
(A)
MU
(u)
MARKER (.7604V , 1.001uA , 19.2E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.21.

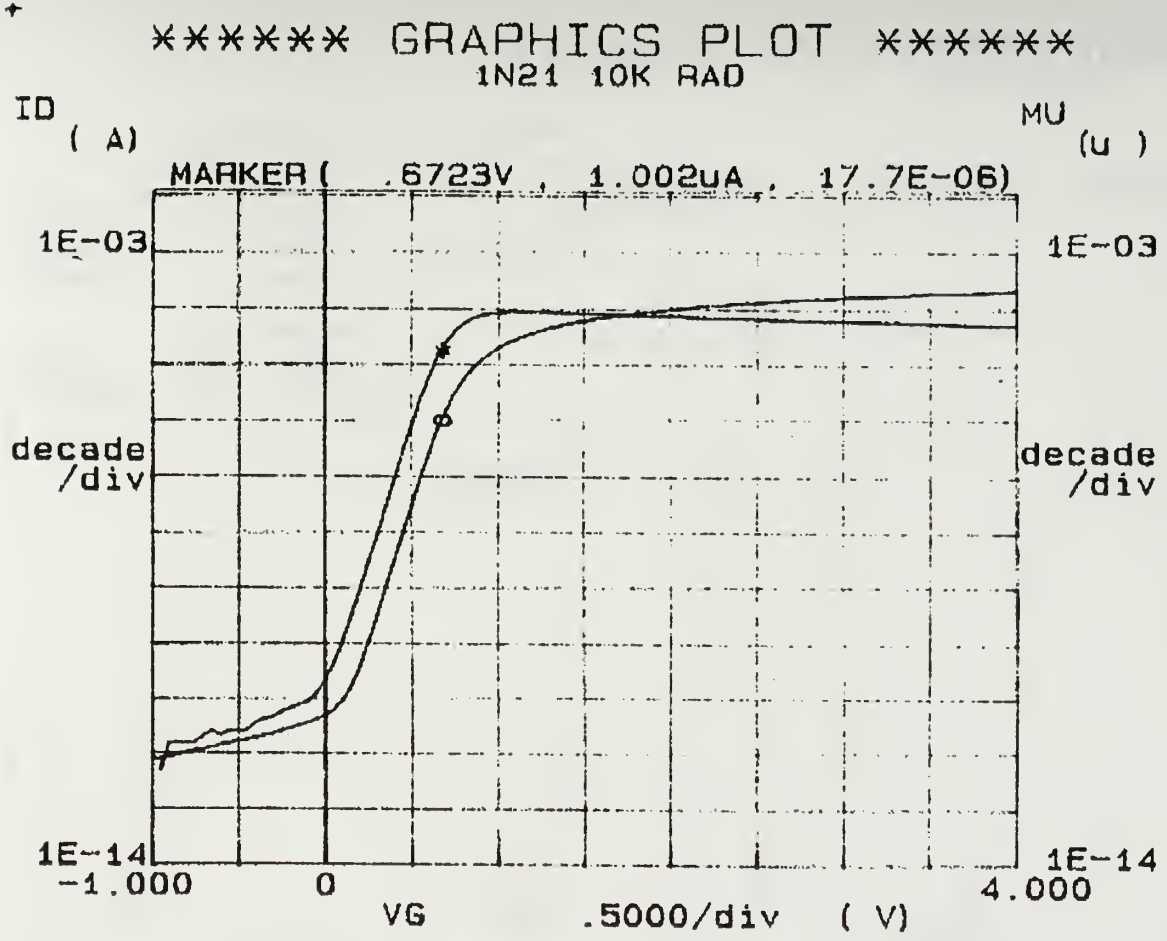

****** GRAPHICS PLOT ******
1N21 10K RAD
ID
(A)
MU
(u)
MARKER (.6723V , 1.002uA , 17.7E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.22.

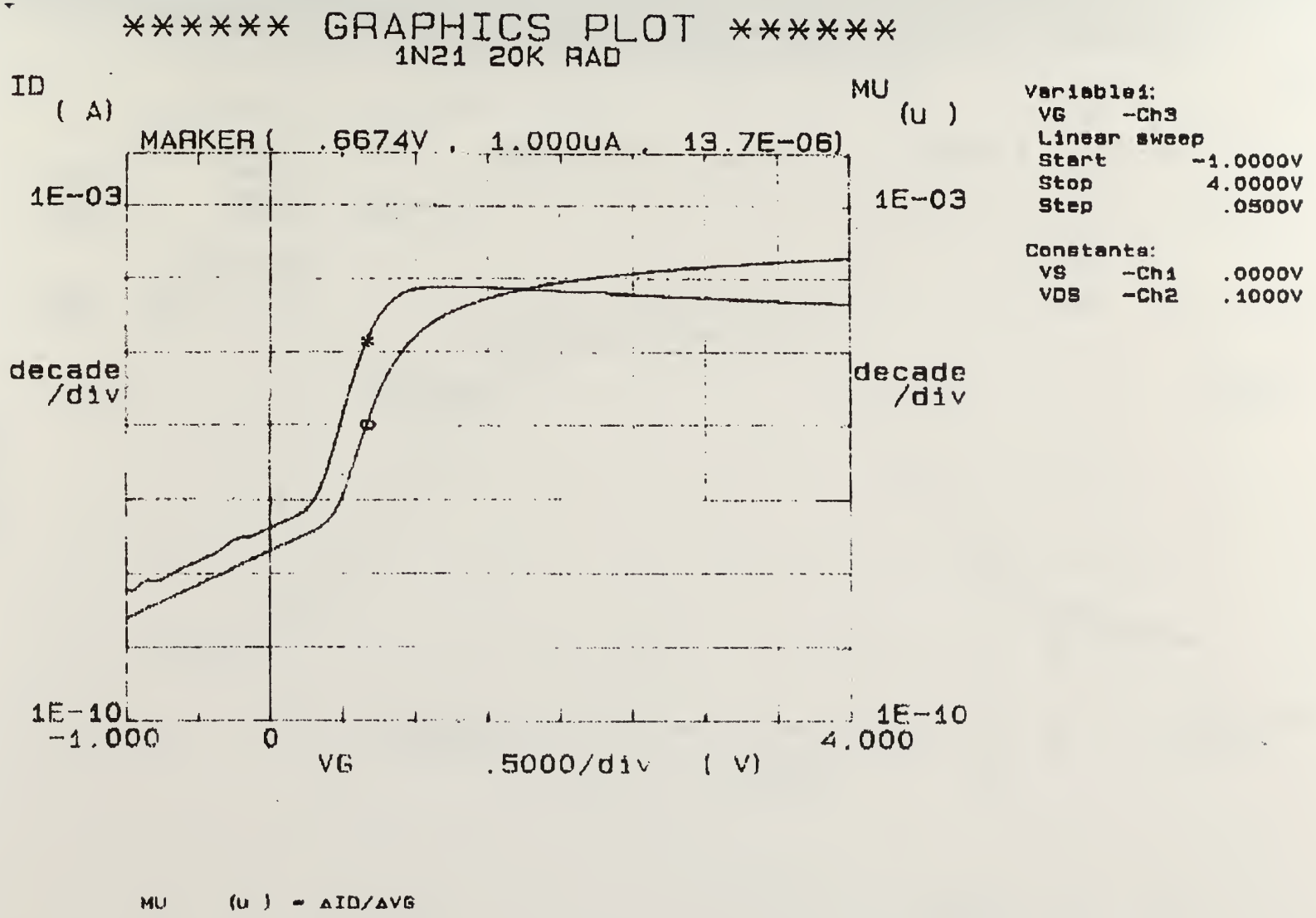

****** GRAPHICS PLOT ******
1N21 20K RAD
ID
(A)
MU
(u)
MARKER (.6674V , 1.000uA , 13.7E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-10
1E-10
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.23.

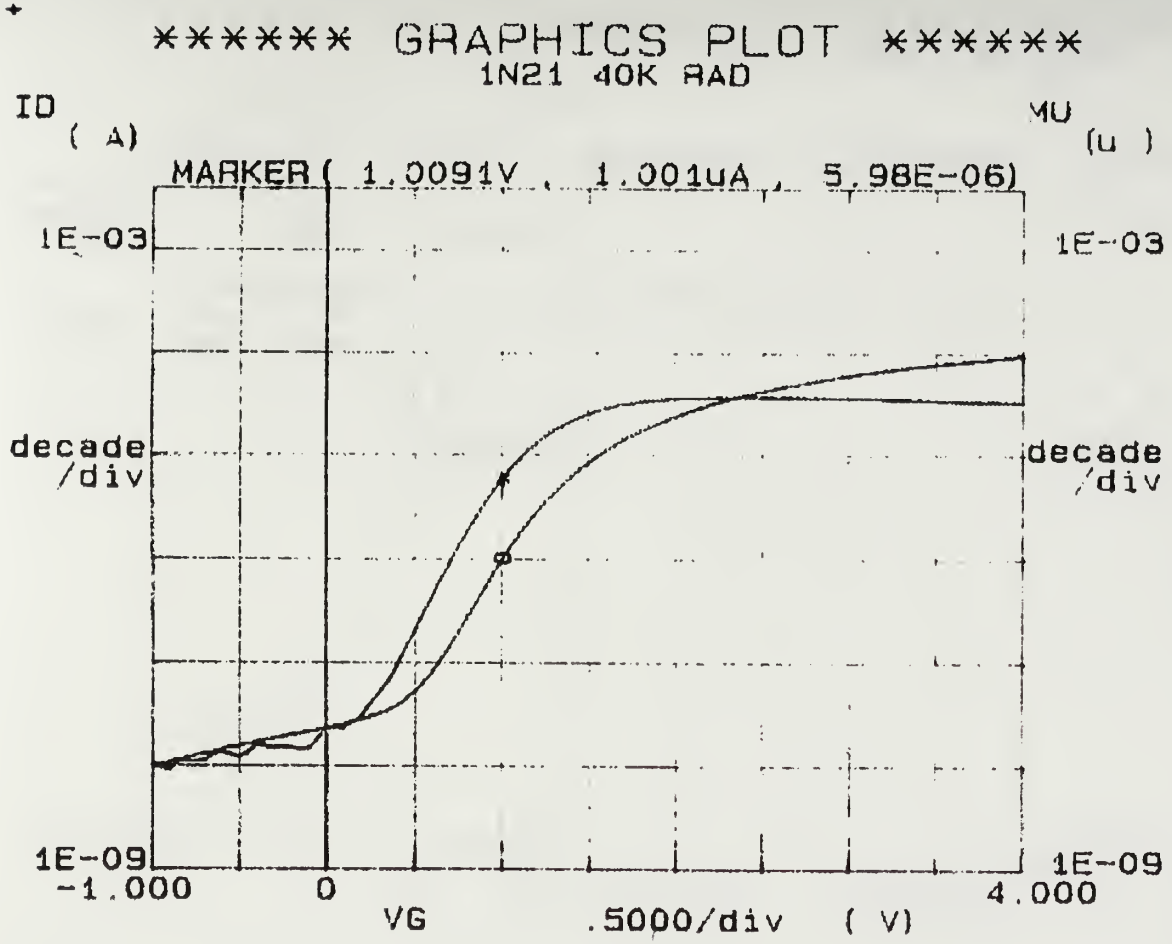

****** GRAPHICS PLOT ******
1N21 40K RAD
ID
(A)
MU
(u)
MARKER (1.0091V , 1.001uA , 5.98E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-09
1E-09
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = AID/AVG

Figure C.24.

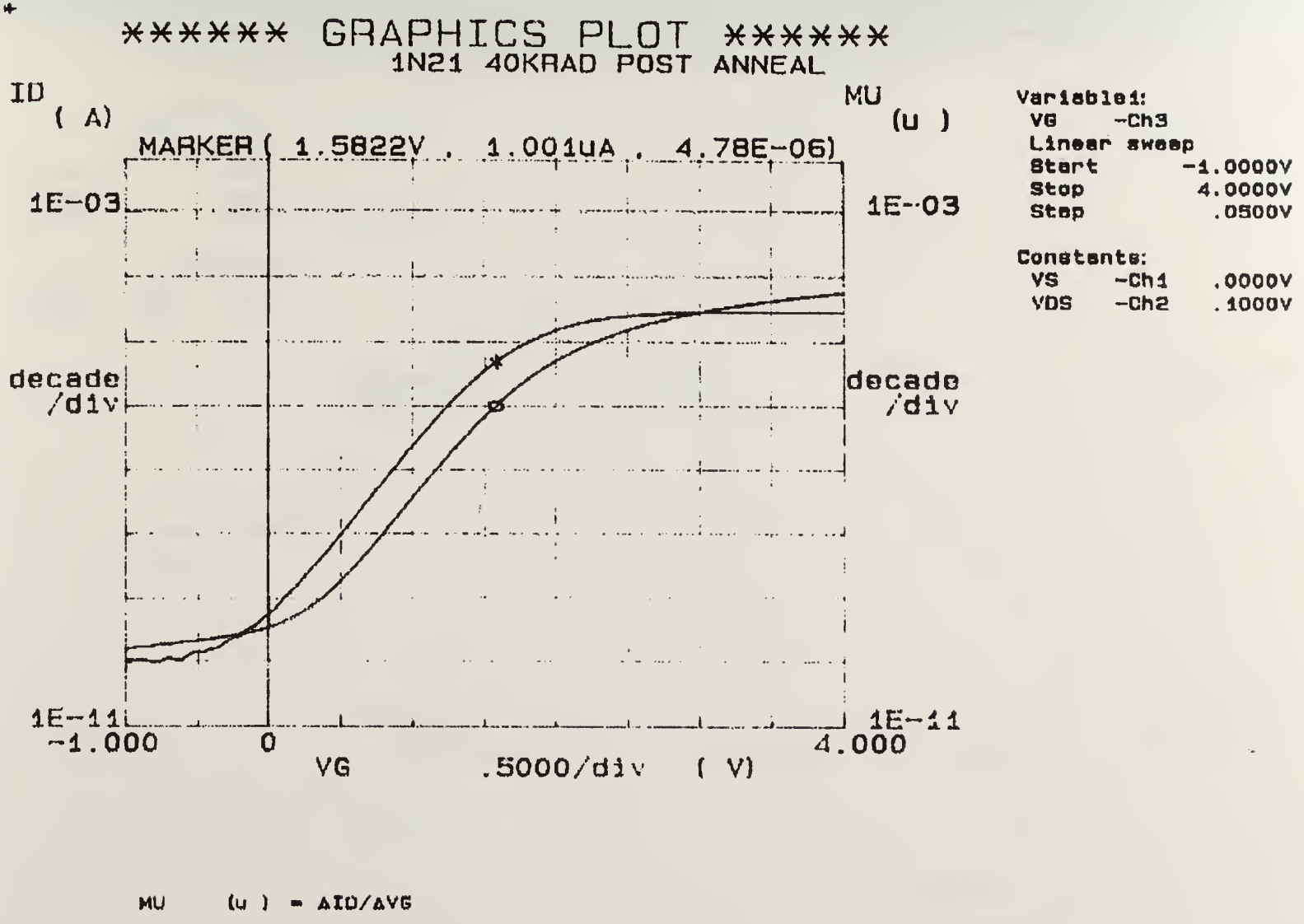

****** GRAPHICS PLOT ******
1N21 40KRAD POST ANNEAL
ID
(A)
MU
(u)
MARKER (1.5822V , 1.001uA , 4.78E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-11
1E-11
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = AID/AVG

Figure C.25.

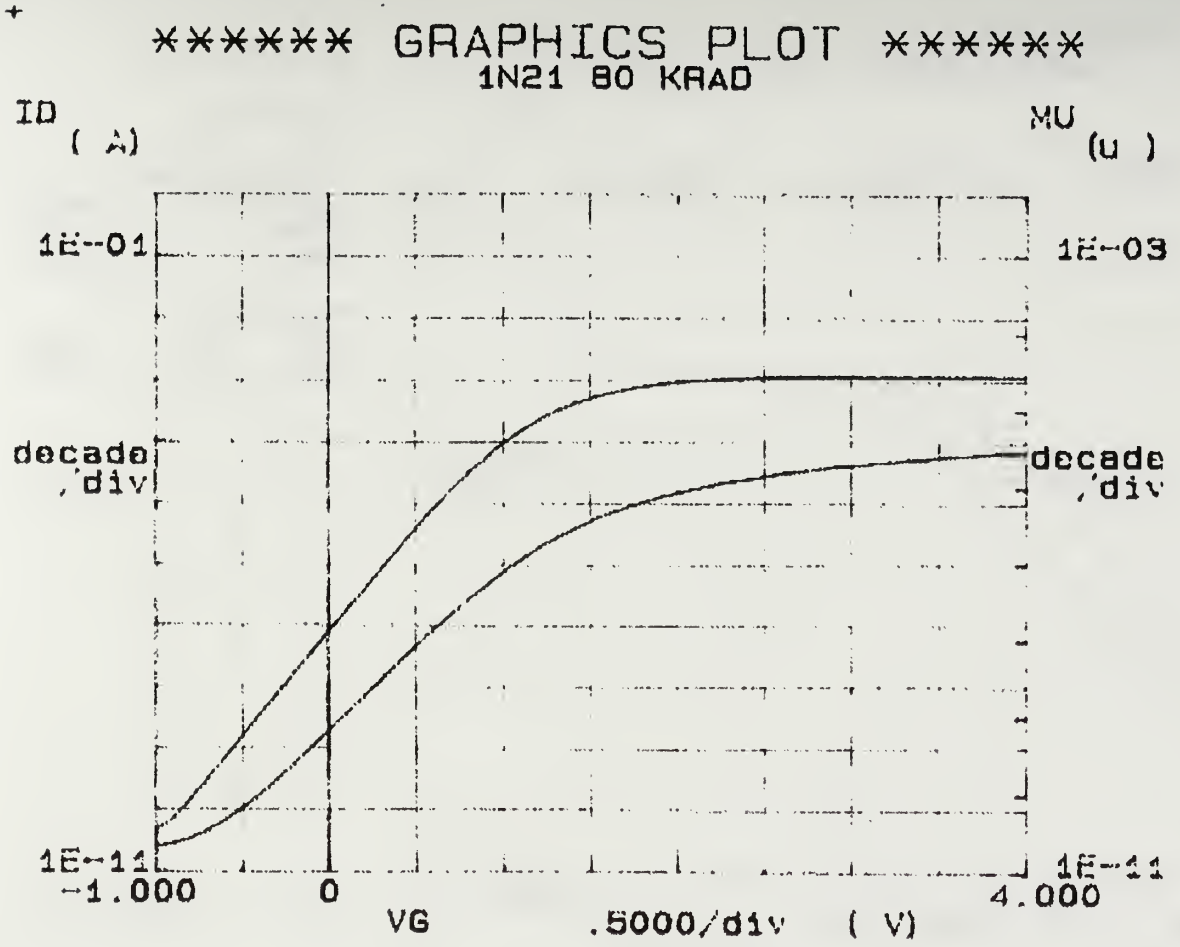

****** GRAPHICS PLOT ******
1N21 80 KRAD
ID
(A)
MU
(u)
1E-01
1E-03
decade
/div
decade
/div
1E-11
1E-11
-1.000
0
4.000
VG
.5000/div
(V)
MU (u) = ΔID/ΔVG
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .1000V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V

Figure C.26.

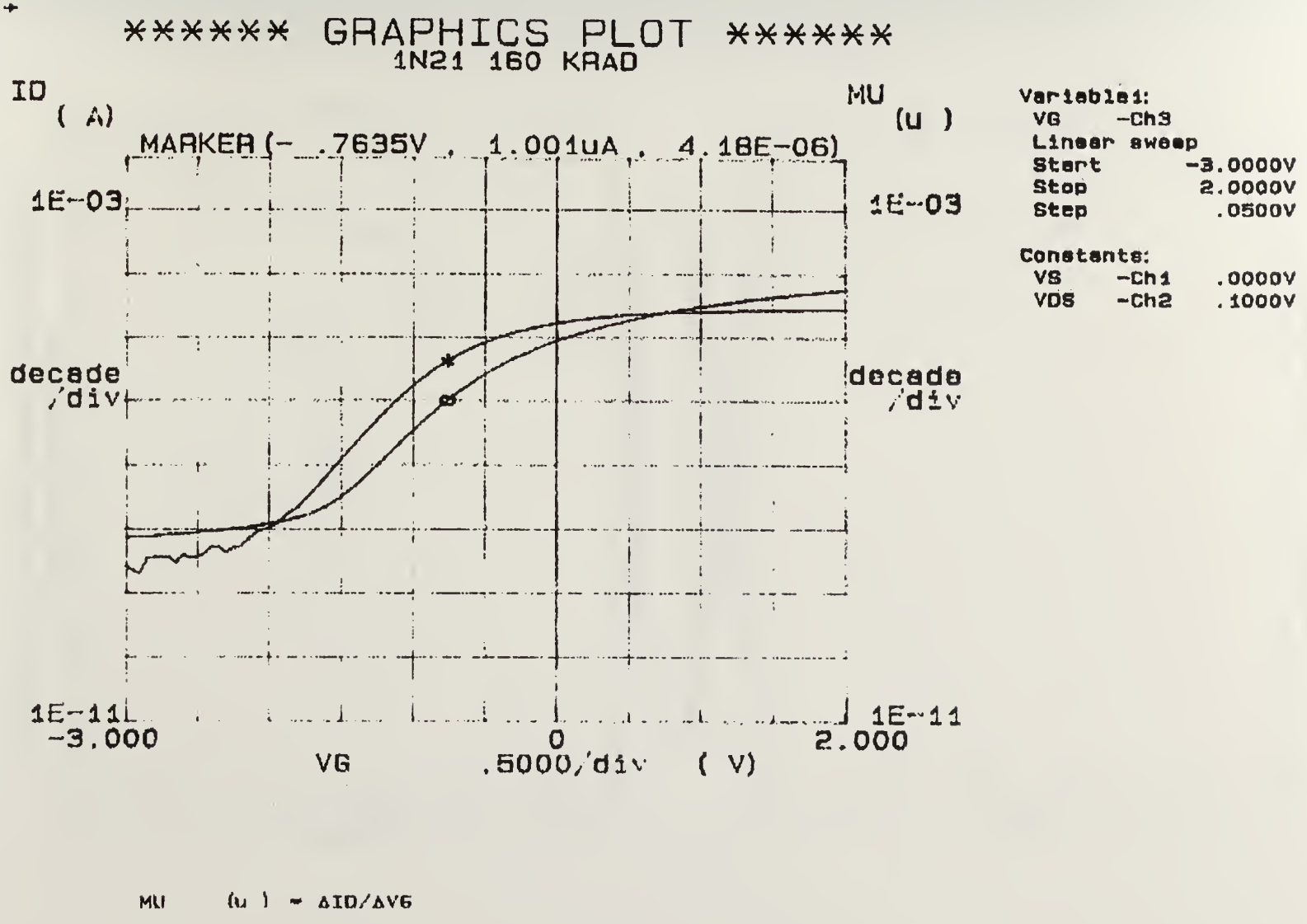

****** GRAPHICS PLOT ******
1N21 160 KRAD
ID
(A)
MU
(u)
MARKER(- .7635V , 1.001uA , 4.18E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-11
1E-11
-3.000
0
2.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.27.

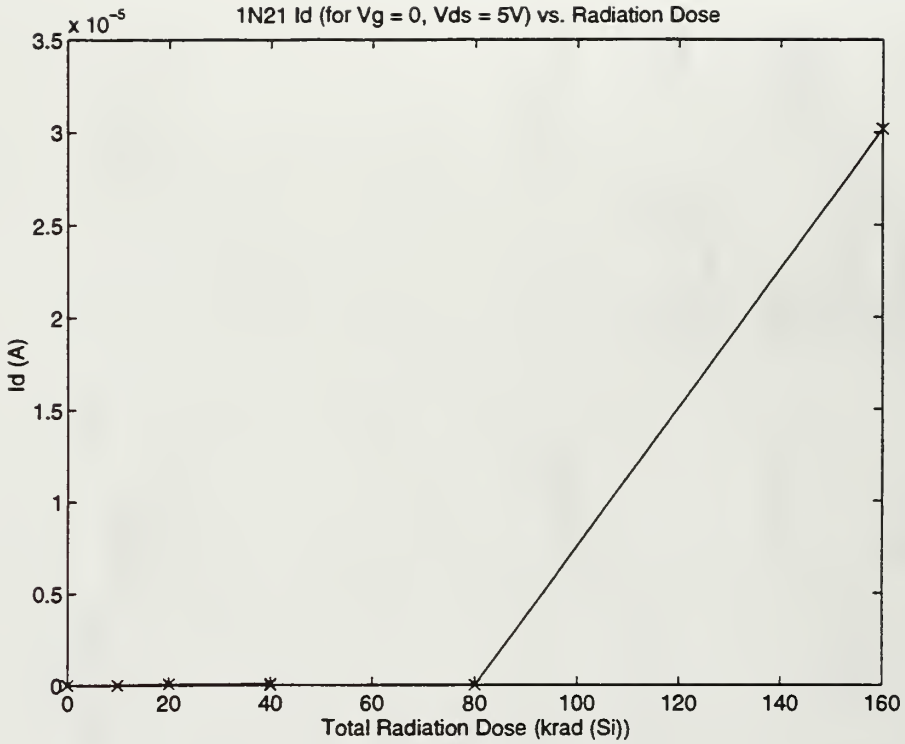


Figure C.28. V_{ds} = 5V Subthreshold Leakage Current.

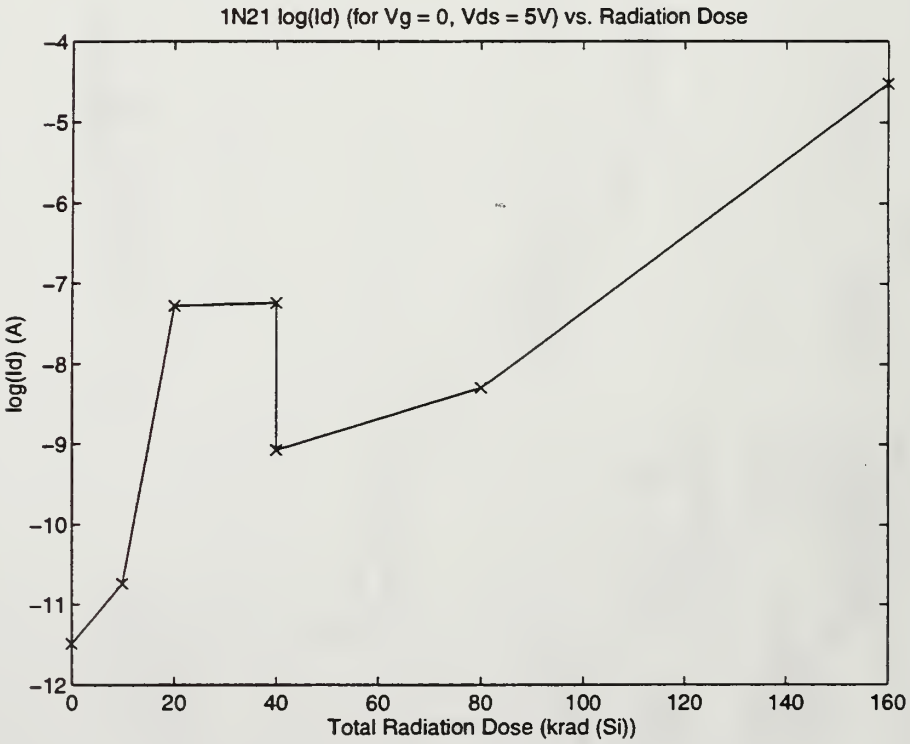


Figure C29. V_{ds} = 5V Subthreshold Leakage Current.

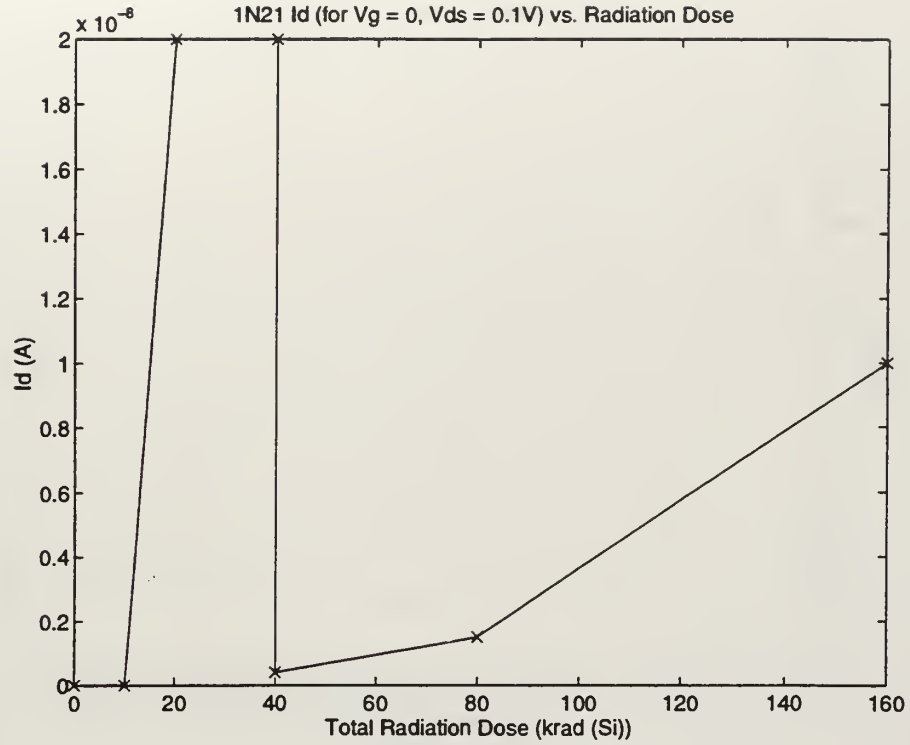


Figure C.30. V_{ds} = 0V Subthreshold Leakage Current.

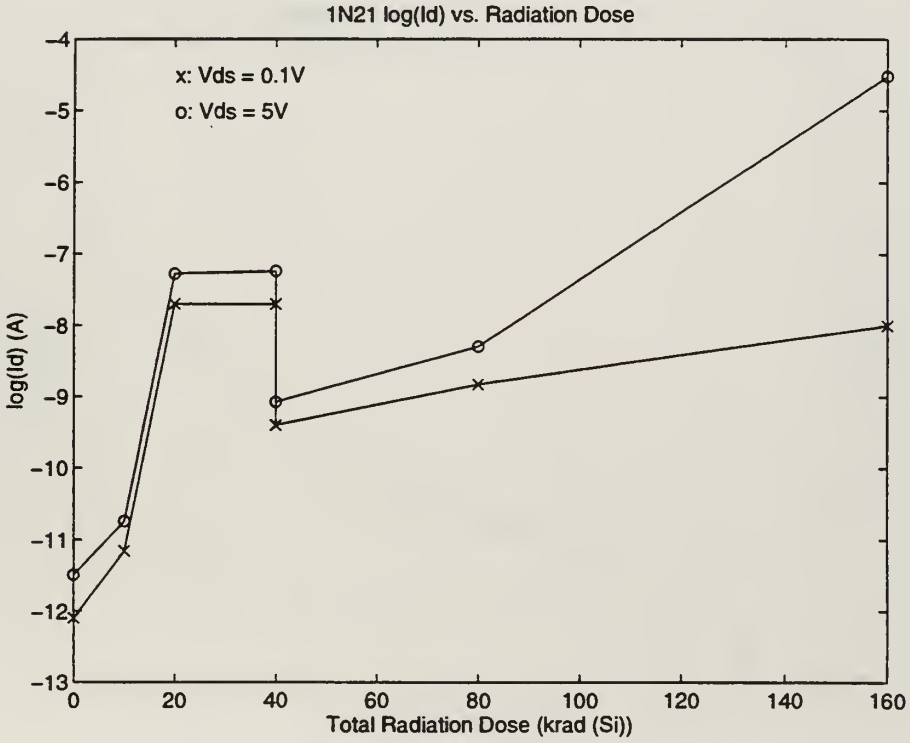


Figure C.31. V_{ds} Subthreshold Leakage Current Comparison.

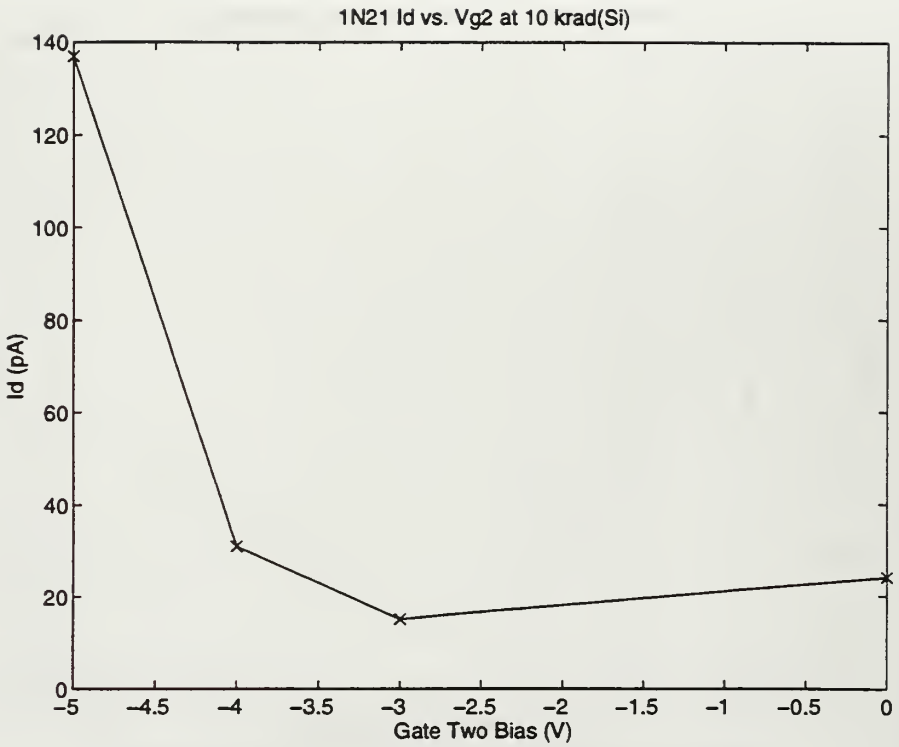


Figure C.32.

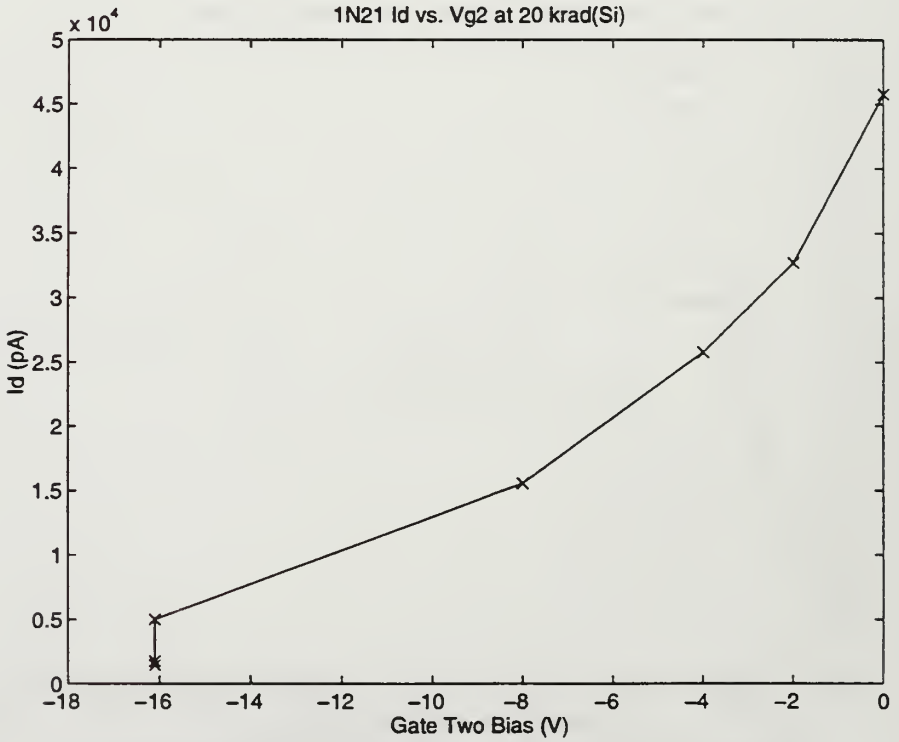


Figure C.33.

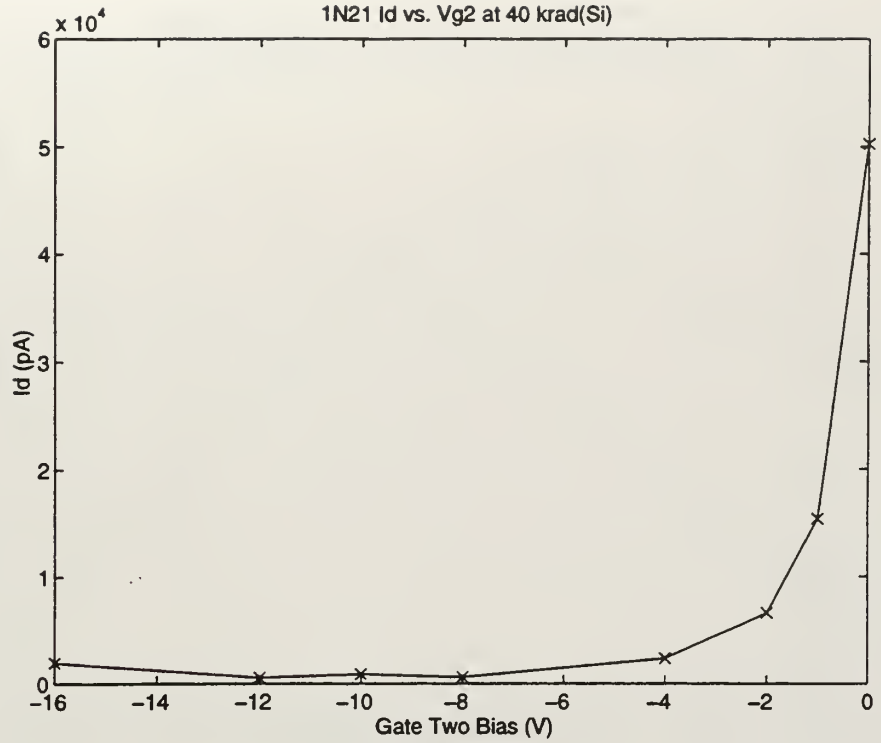


Figure C.34.

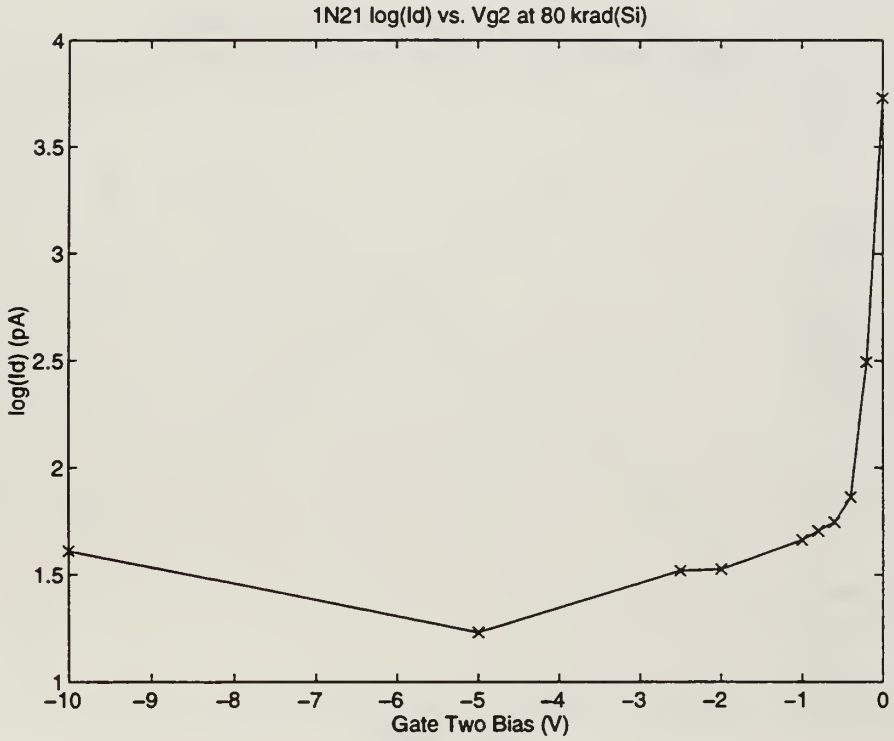


Figure C.35.

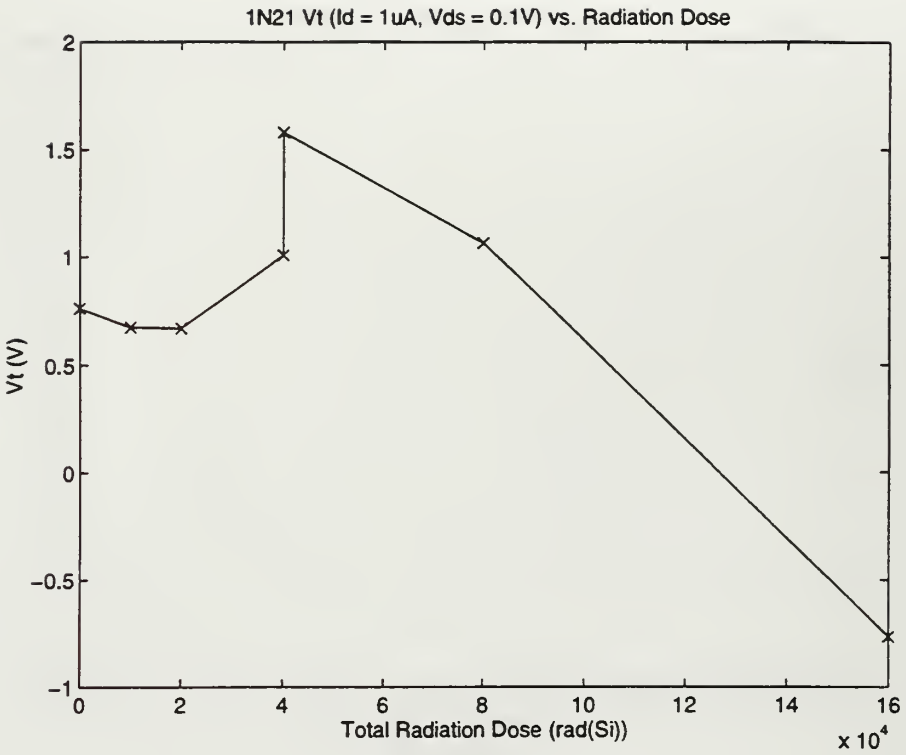


Figure C.36.

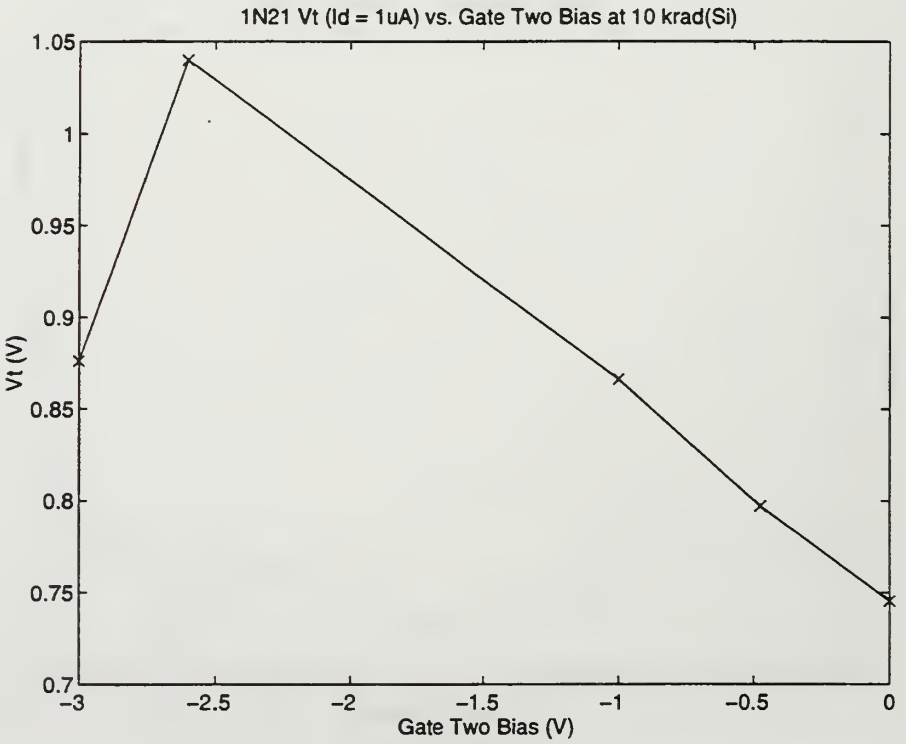


Figure C.37.

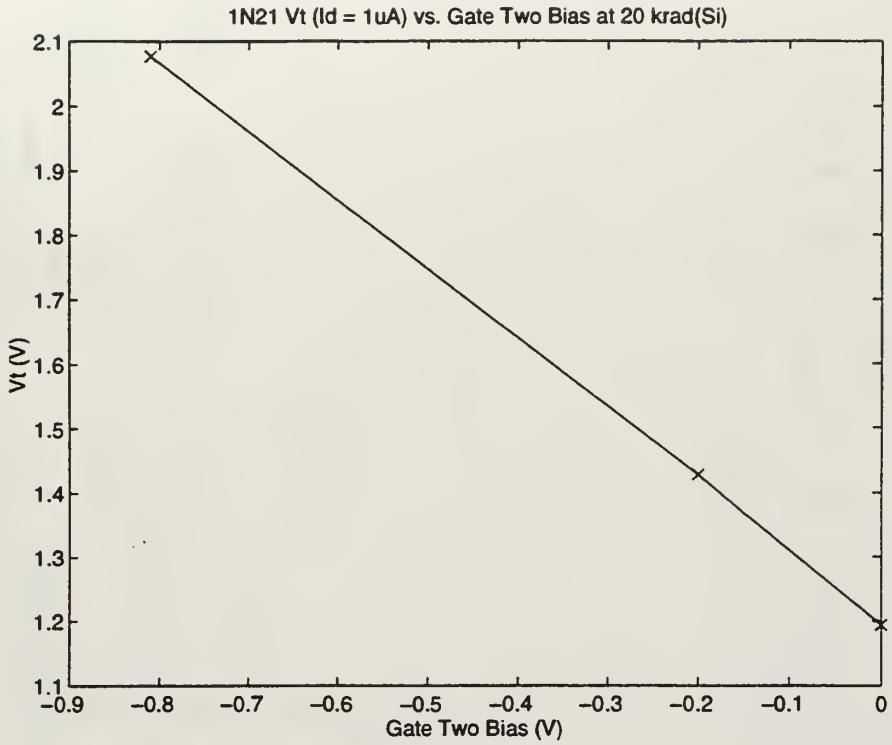


Figure C.38.

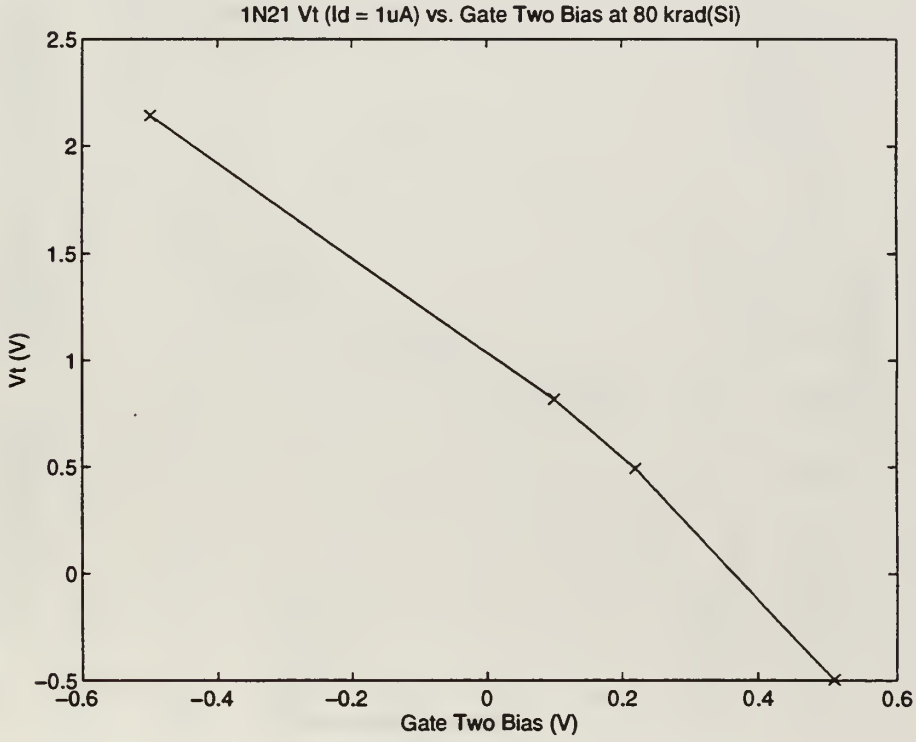


Figure C.39.

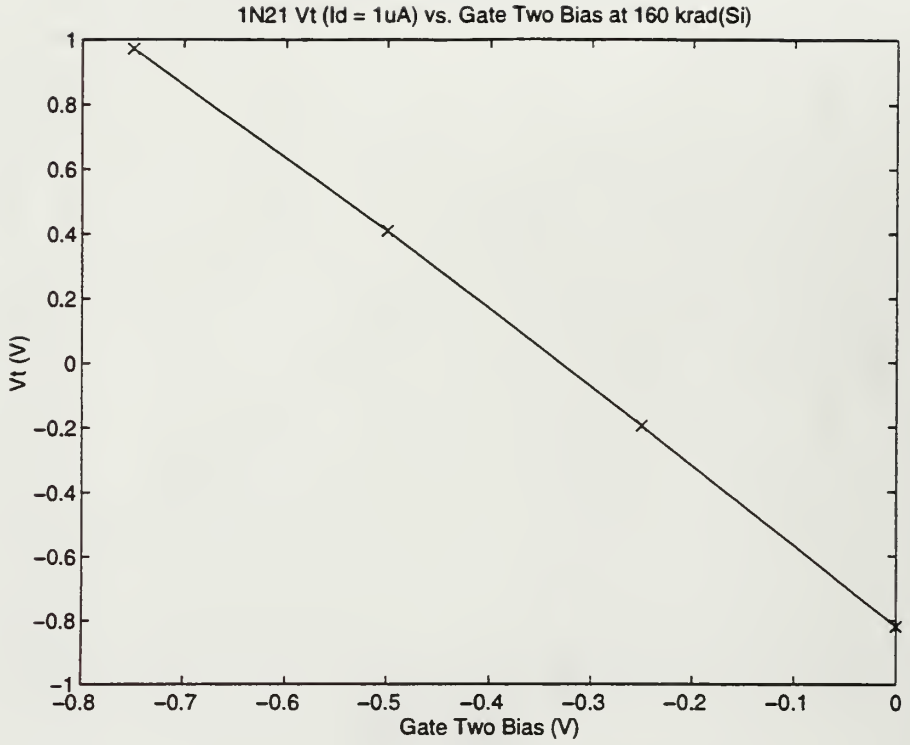


Figure C.40.

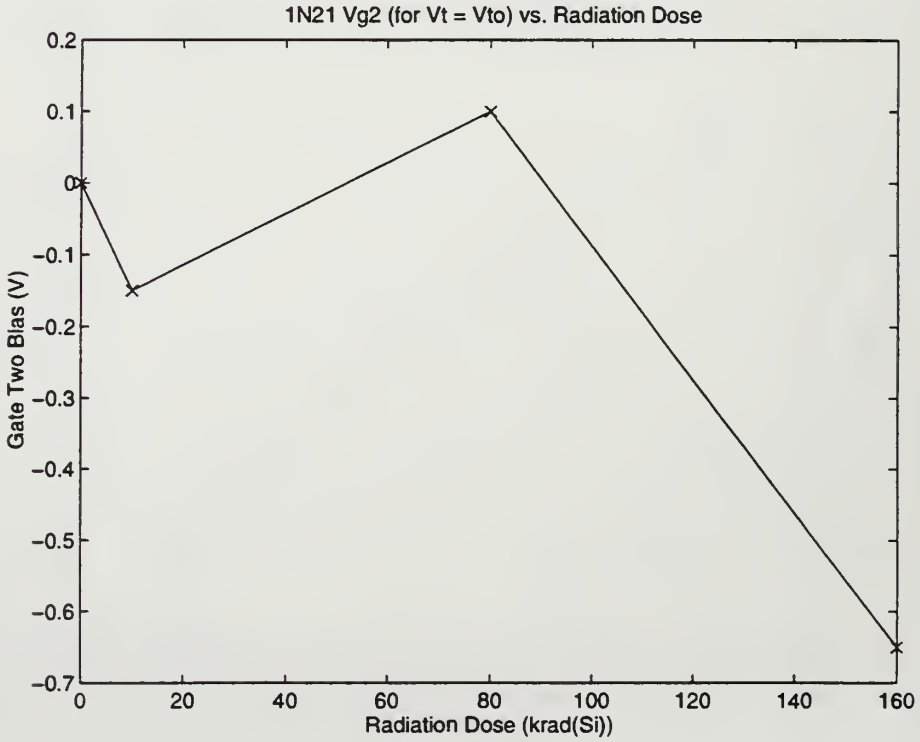
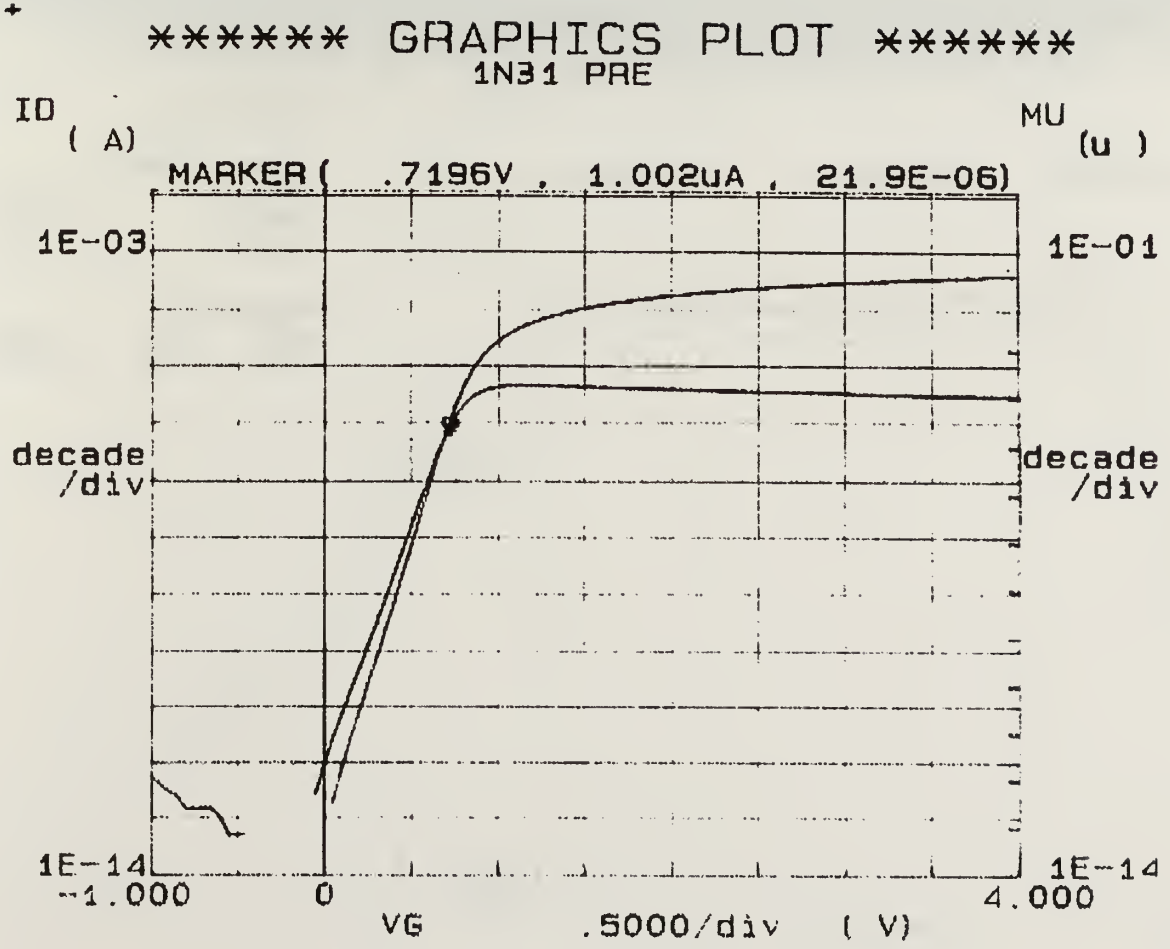


Figure C.41.



Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V

Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V

Figure C.42.

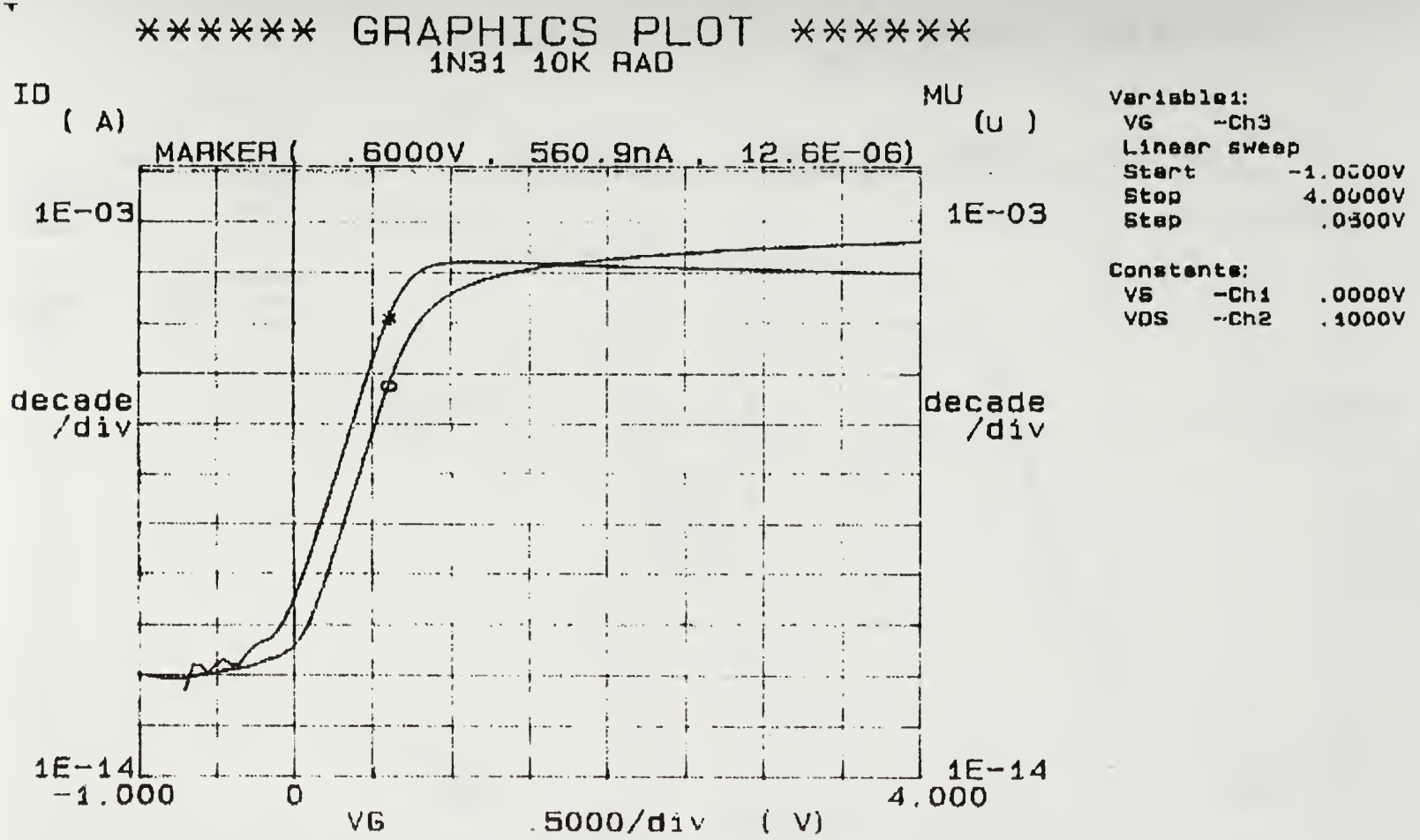

****** GRAPHICS PLOT ******
1N31 10K RAD
ID
(A)
MU
(u)
MARKER (.6000V , 560.9nA , 12.6E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.43.

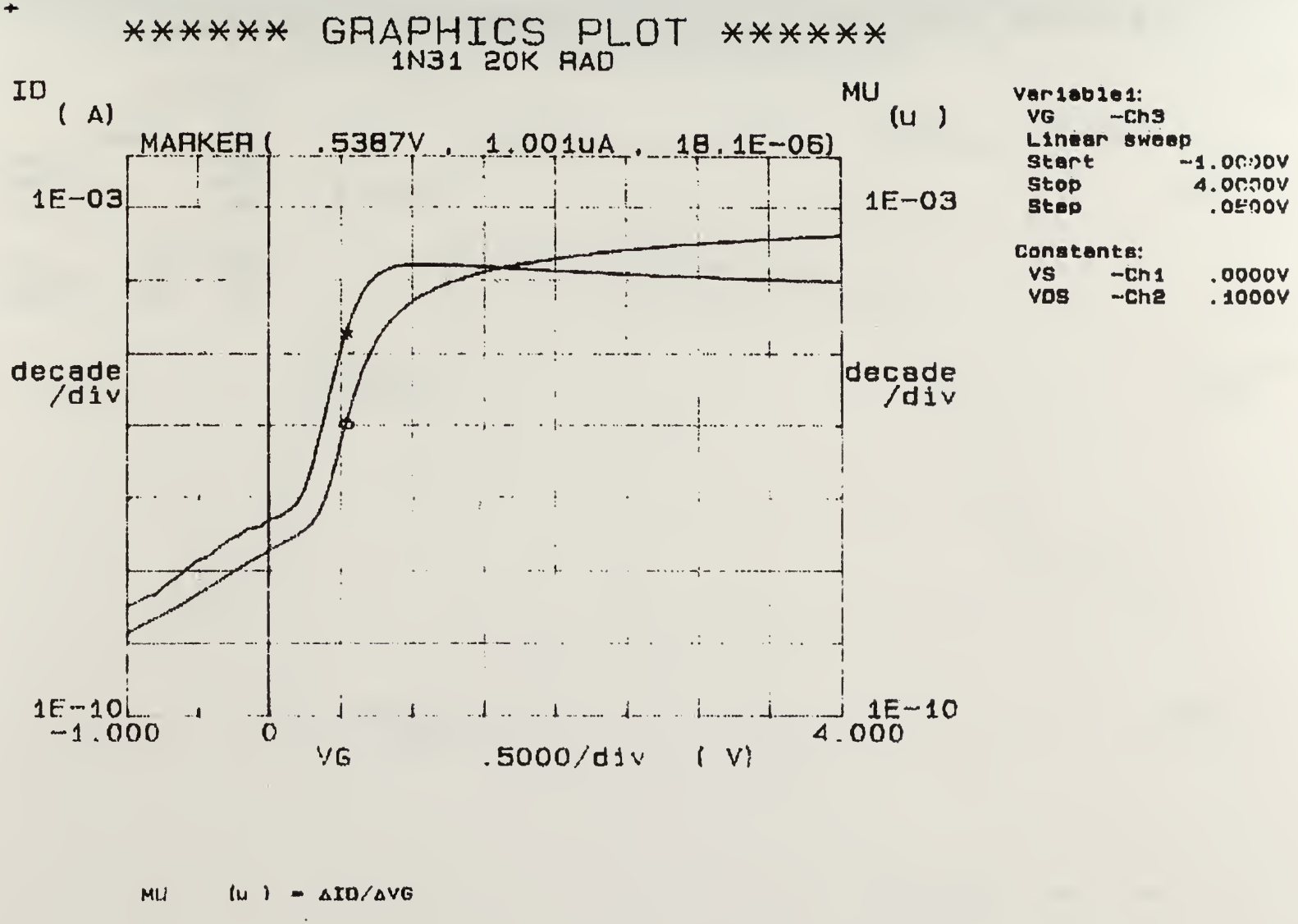

****** GRAPHICS PLOT ******
1N31 20K RAD
ID
(A)
MU
(u)
MARKER(.5387V , 1.001uA , 18.1E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-10
1E-10
-1.000
0
4.000
VG .5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.44.

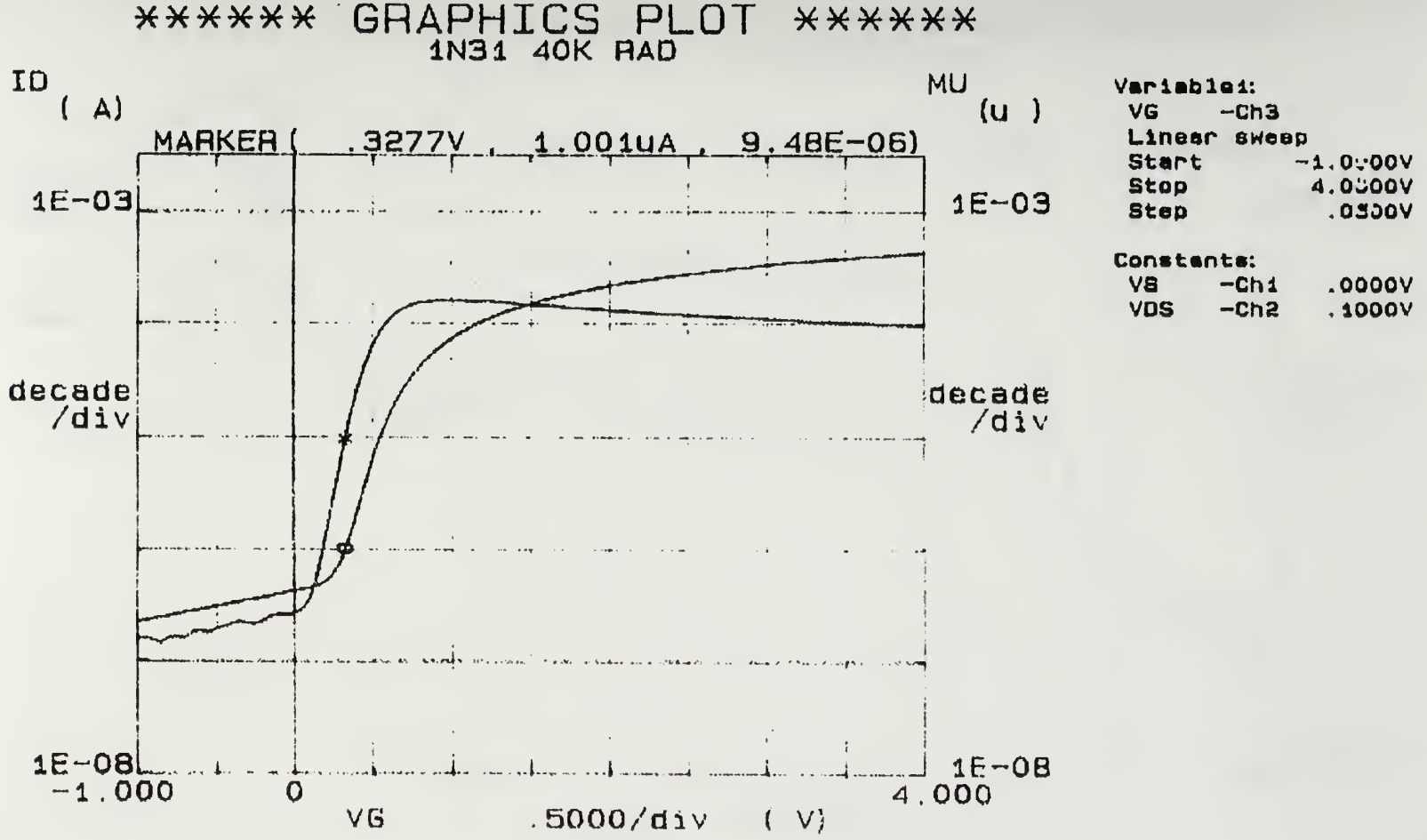

****** GRAPHICS PLOT ******
1N31 40K RAD
ID
(A)
MU
(u)
MARKER (.3277V , 1.001uA , 9.48E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-08
1E-08
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sWeep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VB -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.45.

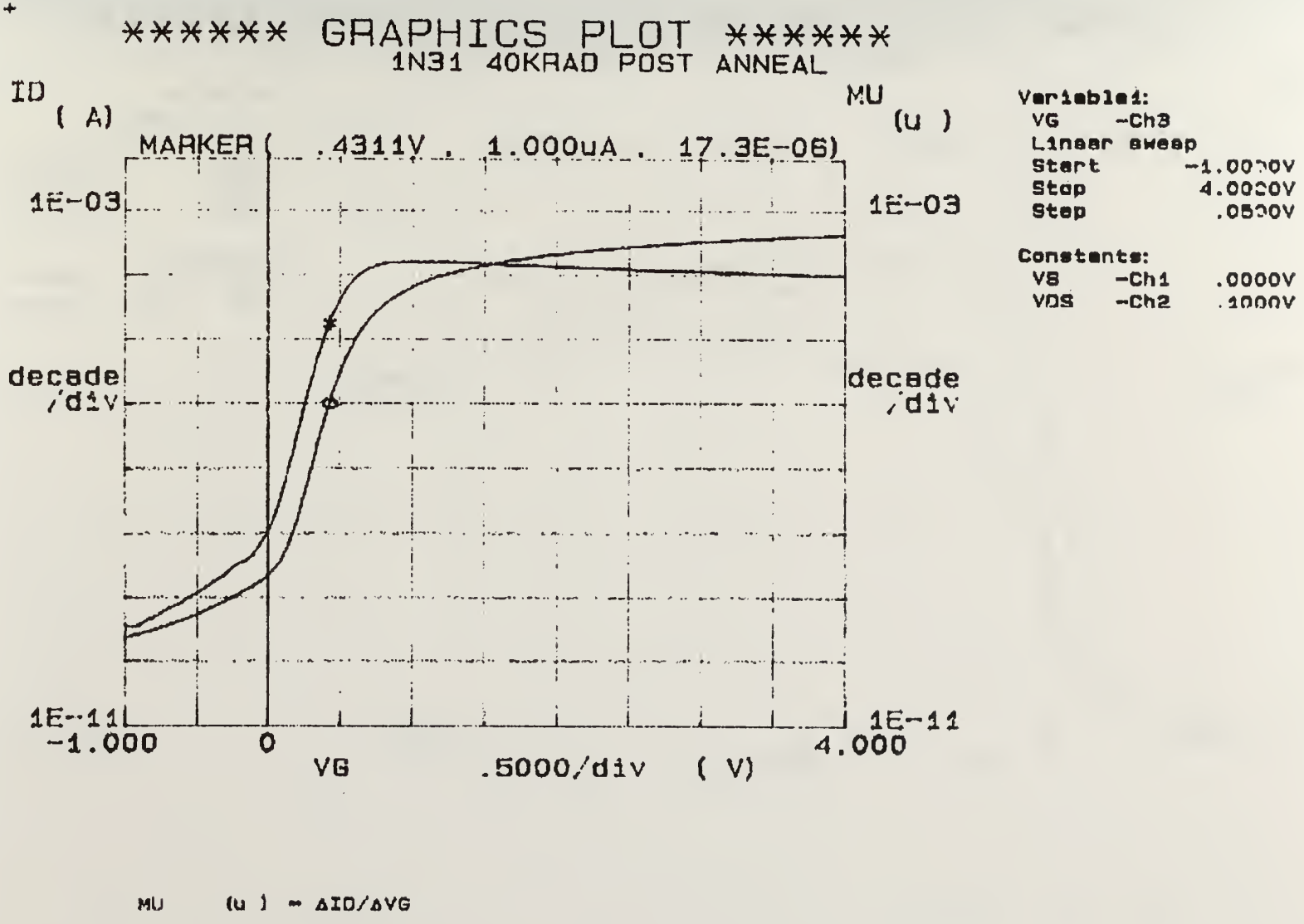

****** GRAPHICS PLOT ******
1N31 40KRAD POST ANNEAL
ID
(A)
MU
(u)
MARKER (.4311V , 1.000uA , 17.3E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-11
1E-11
-1.000
0
4.000
VG .5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VB -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.46.

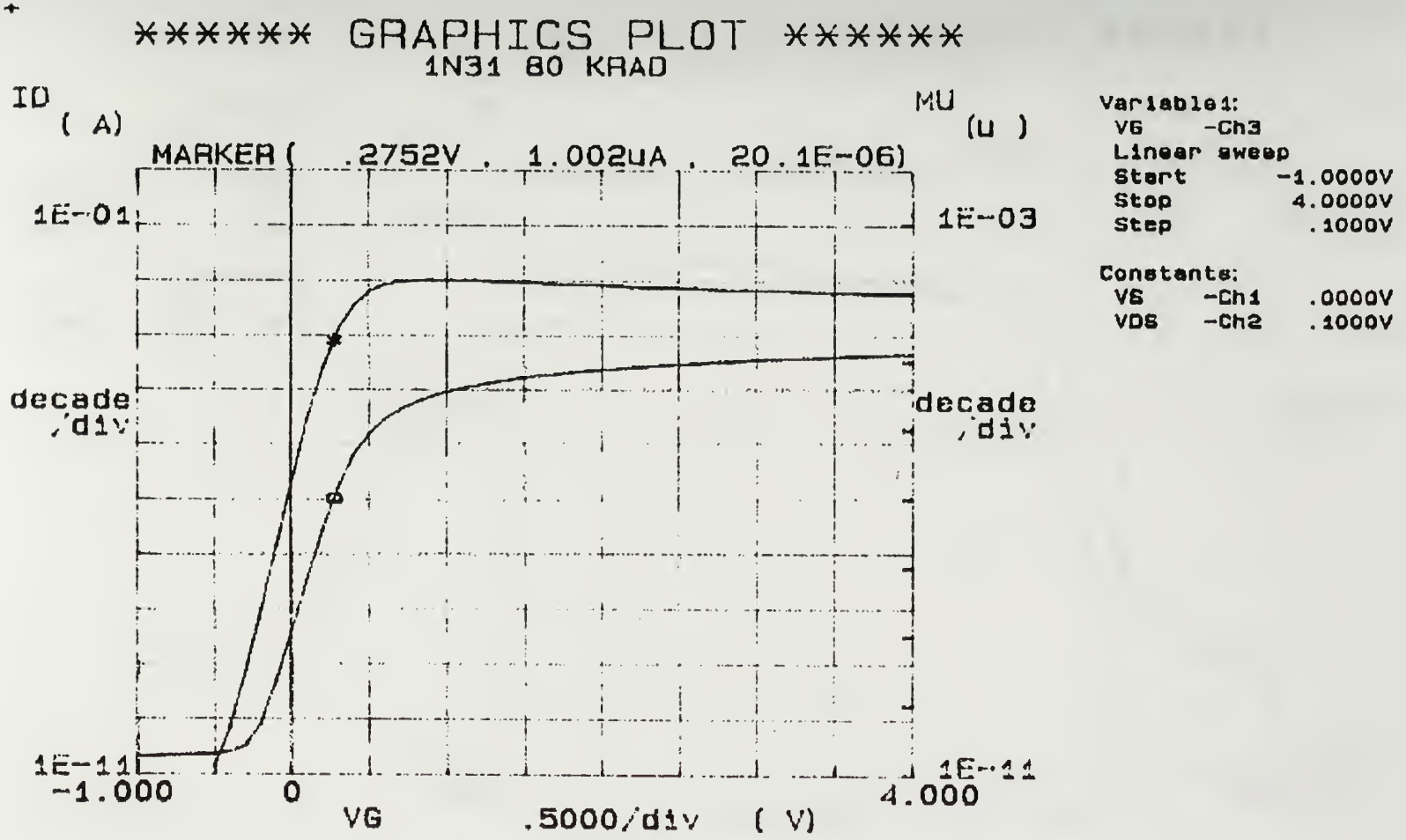

****** GRAPHICS PLOT ******
1N31 80 KRAD
ID
(A)
MU
(u)
MARKER (.2752V , 1.002uA , 20.1E-06)
1E-01
1E-03
decade
/div
decade
/div
1E-11
1E-11
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .1000V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.47.

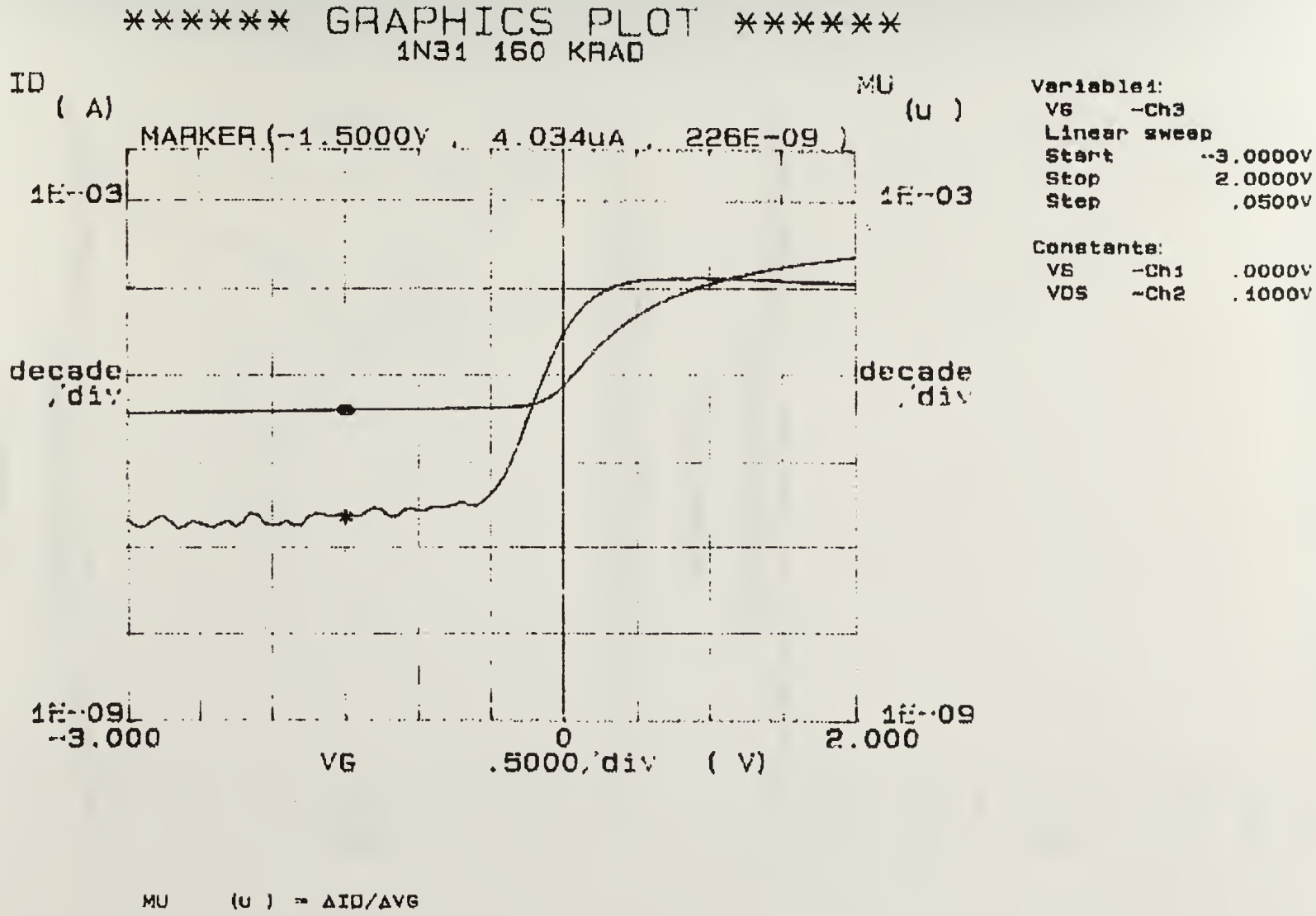

****** GRAPHICS PLOT ******
1N31 160 KRAD
ID
(A)
MU
(u)
MARKER (-1.5000V , 4.034uA , 226E-09)
1E-03
1E-03
decade
/div
decade
/div
1E-09
1E-09
-3.000
0
2.000
VG
.5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V
Constants:
VB -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.48.

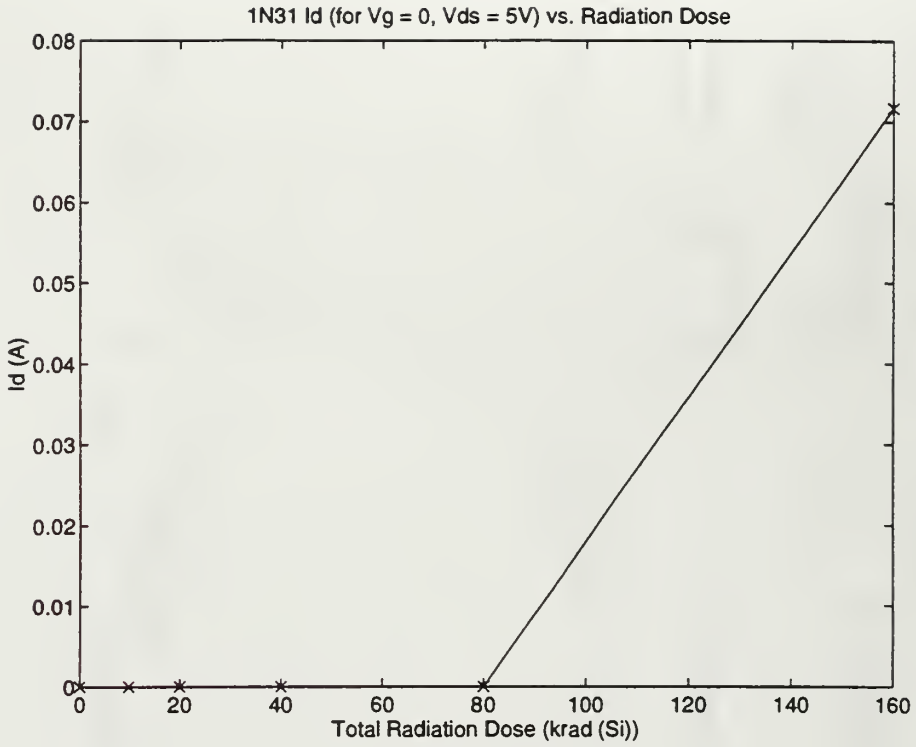


Figure C.49.

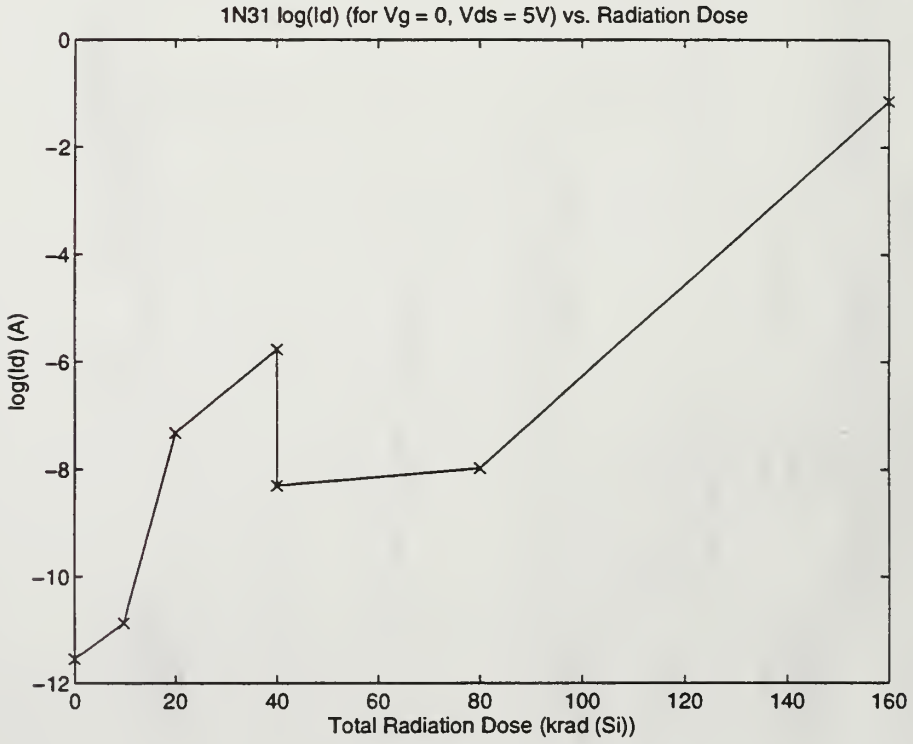


Figure C.50.

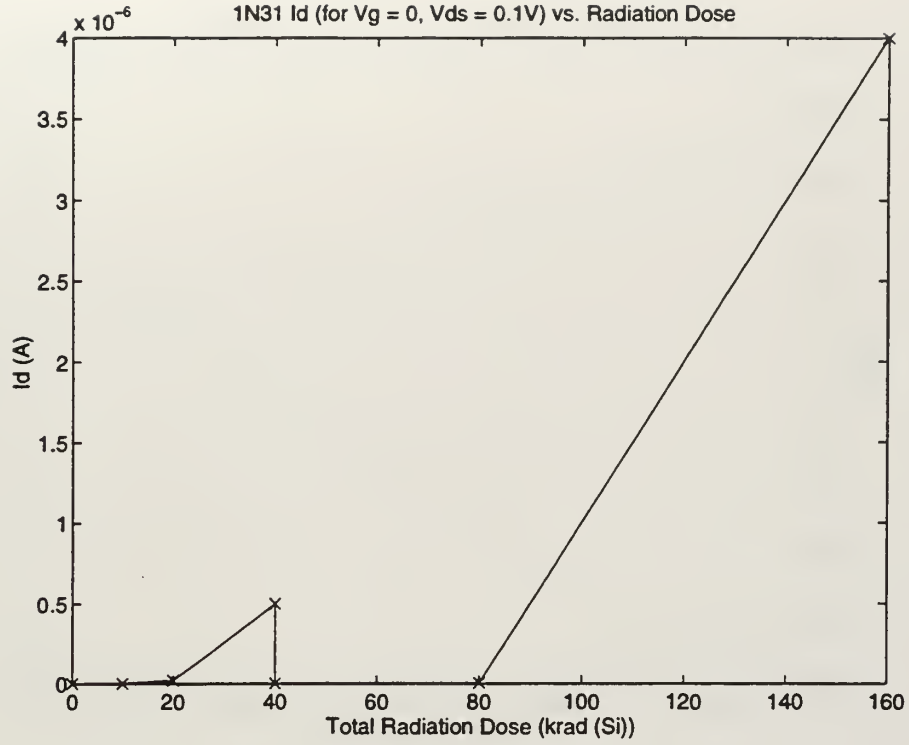


Figure C.51.

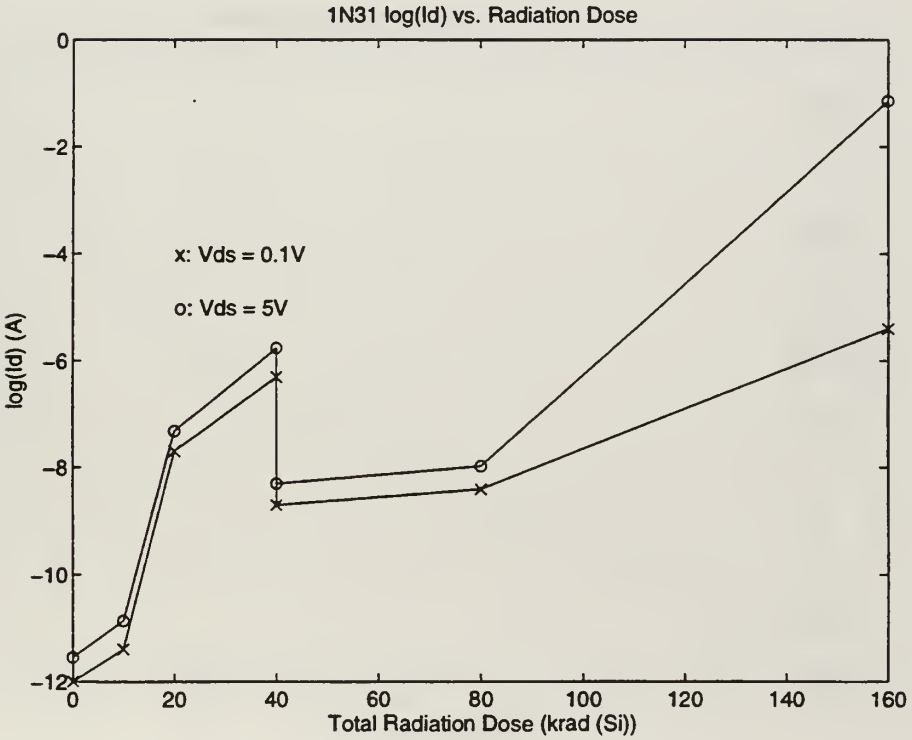


Figure C.52.

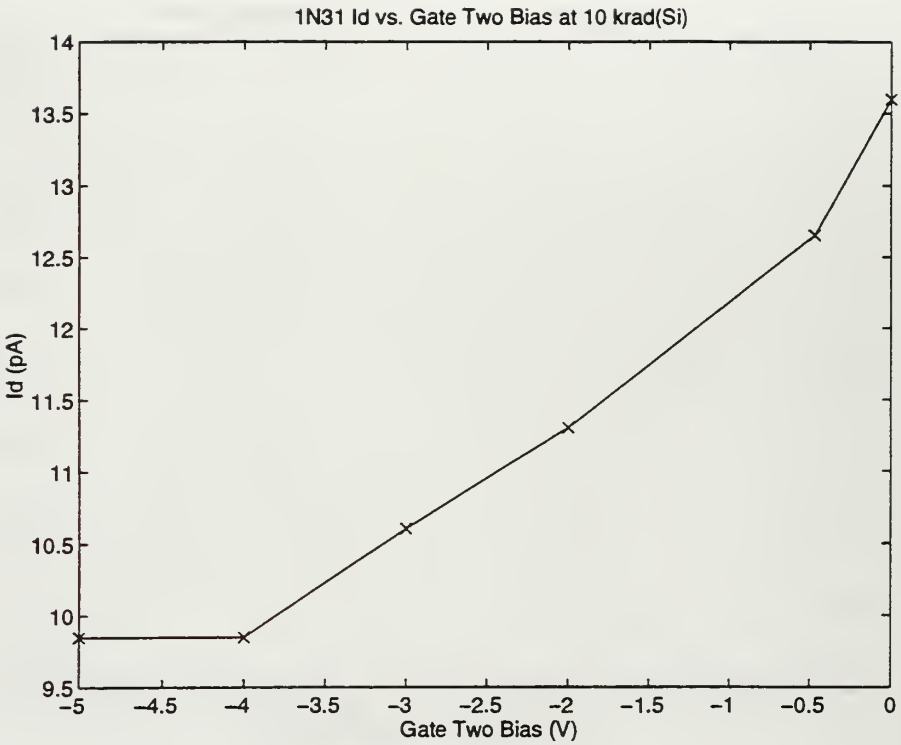


Figure C.53.

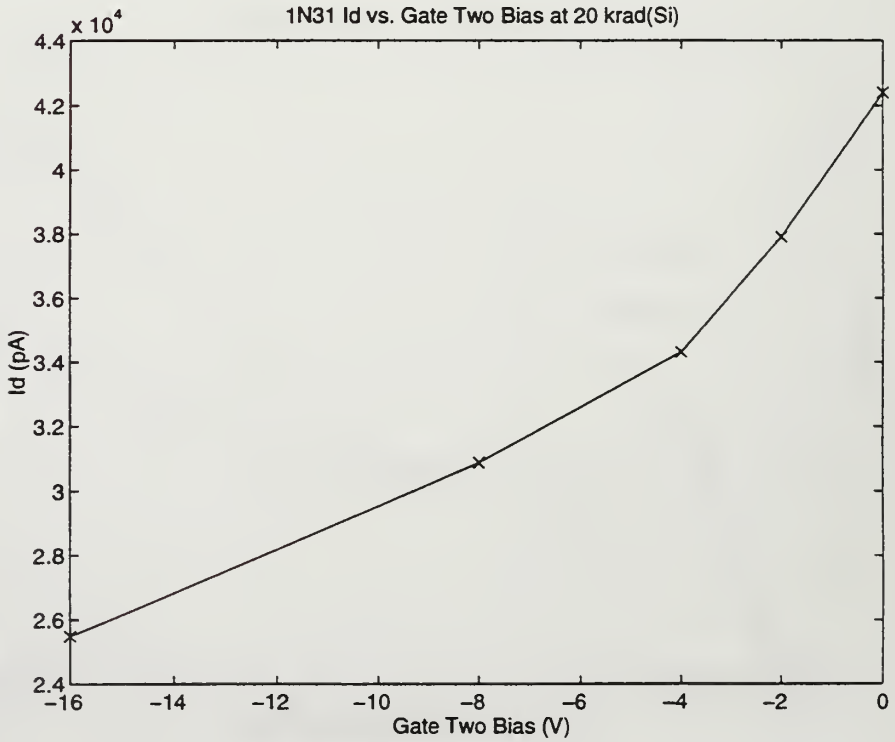


Figure C.54.

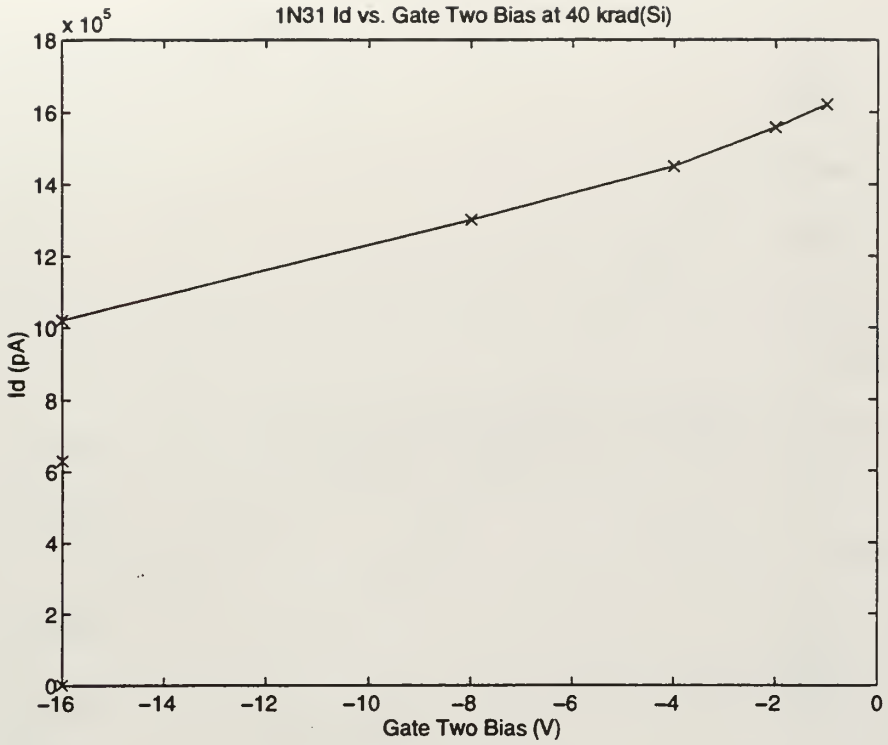


Figure C.55.

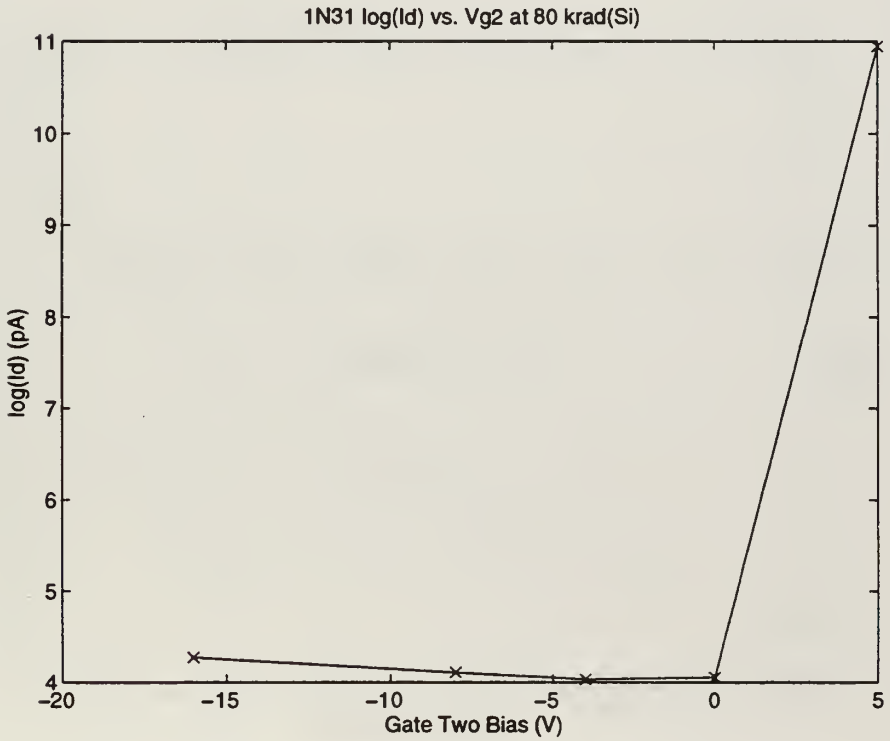


Figure C.56.

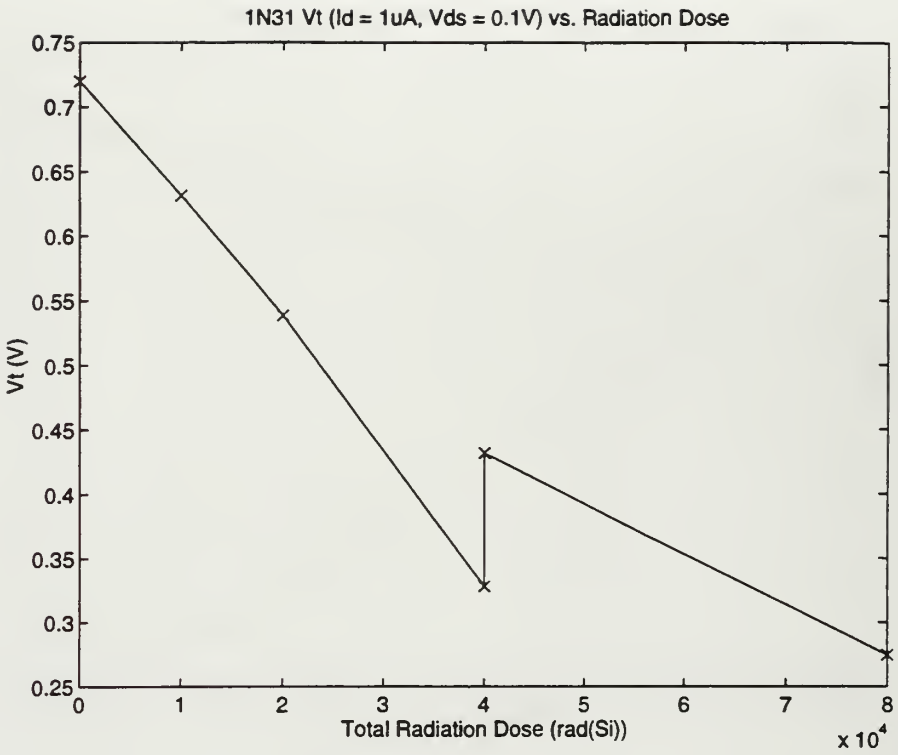


Figure C.57.

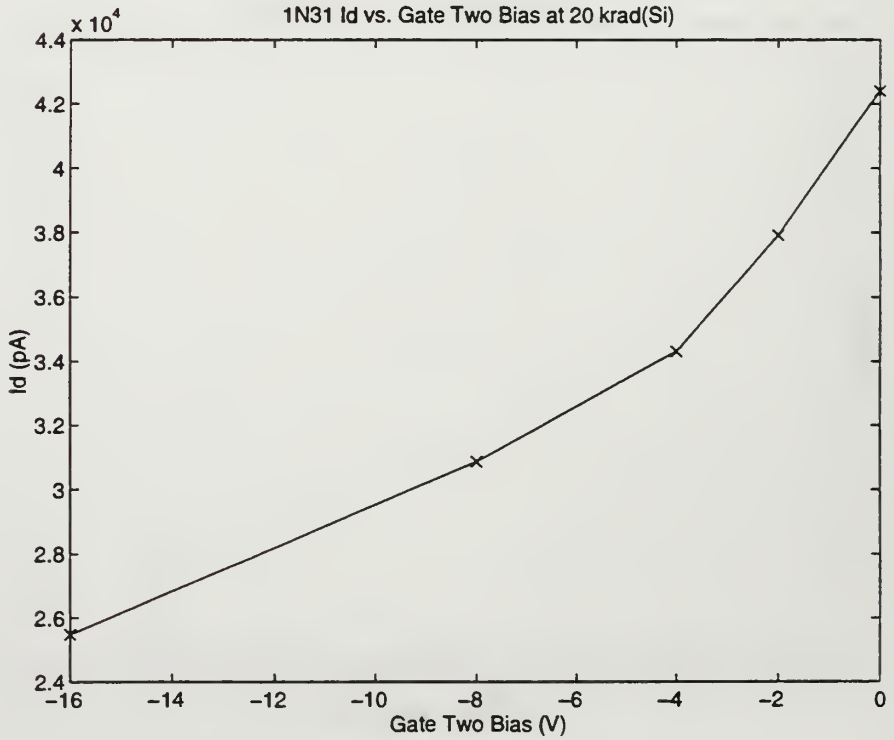


Figure C.58.

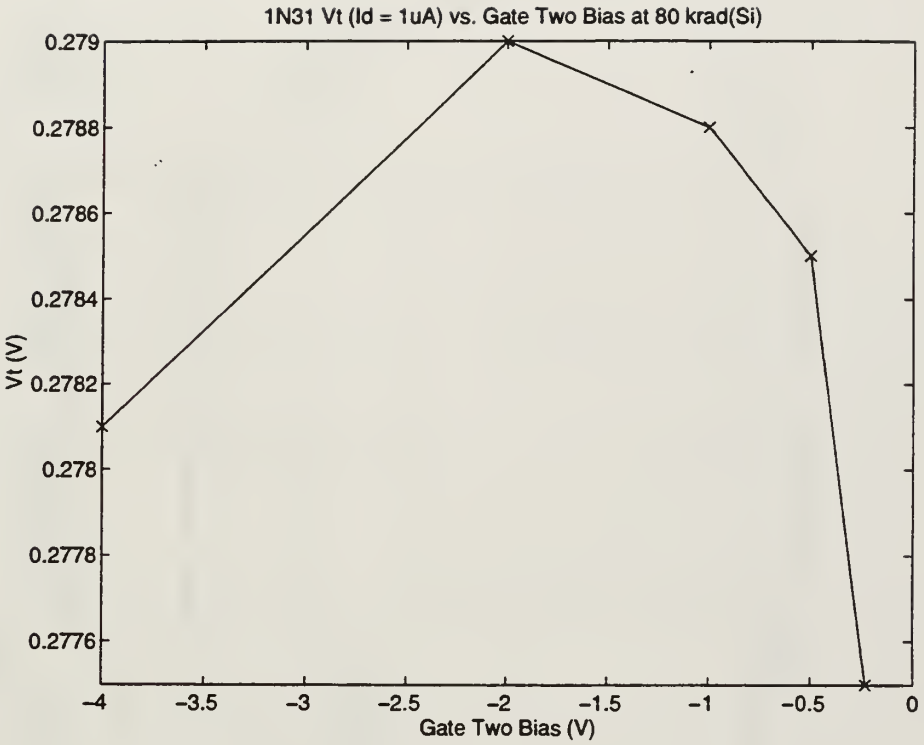
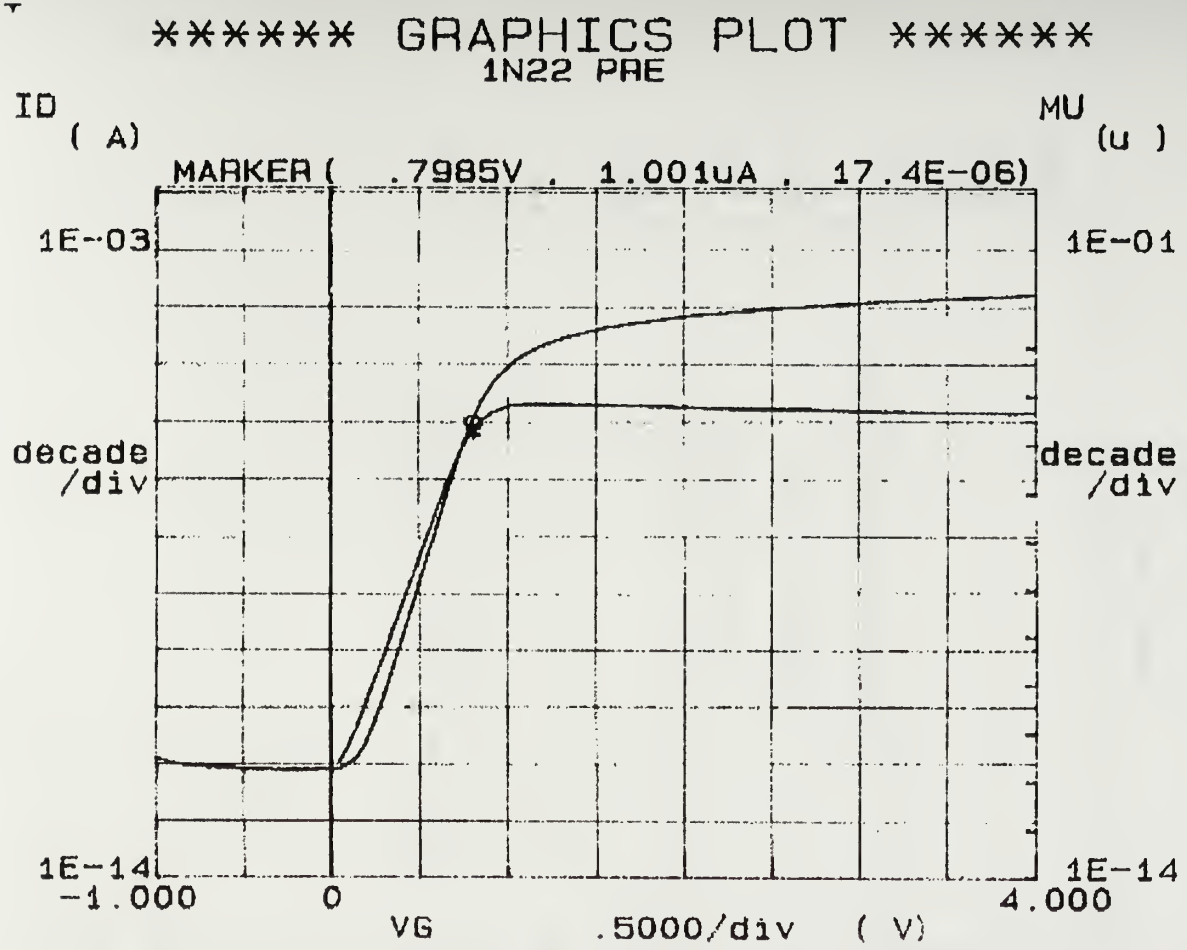

1N31 Vt (Id = 1uA) vs. Gate Two Bias at 80 krad(Si)
Vt (V)
0.279
0.2788
0.2786
0.2784
0.2782
0.278
0.2778
0.2776
-4
-3.5
-3
-2.5
-2
-1.5
-1
-0.5
0
Gate Two Bias (V)

Figure C.59.



Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V

Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V

Figure C.60.

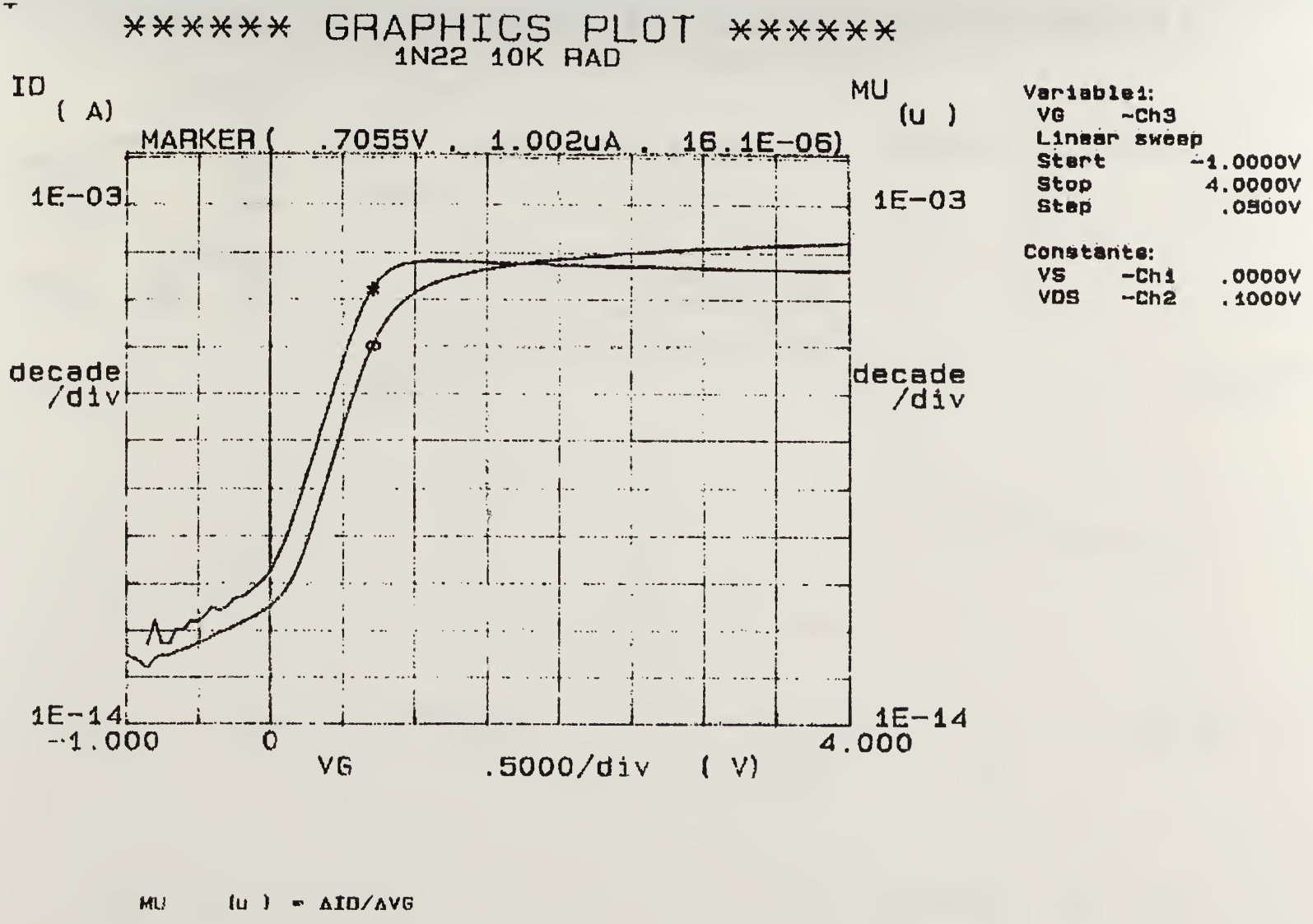
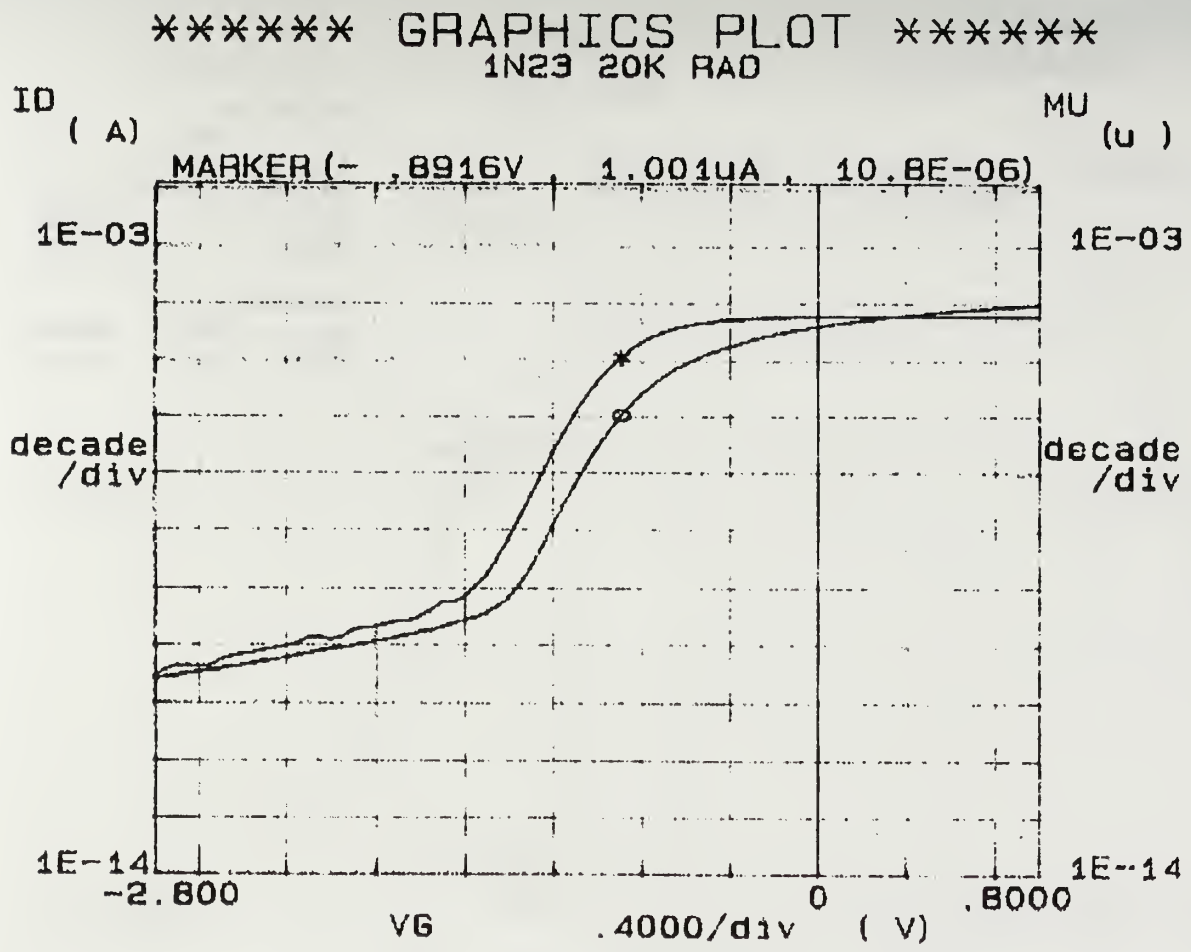

****** GRAPHICS PLOT ******
1N22 10K RAD
ID
(A)
MU
(u)
MARKER(.7055V , 1.002uA , 16.1E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constante:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.61.



Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 1.0000V
Step .0500V

Constants:
VG -Ch1 .0000V
VDS -Ch2 .1000V

Figure C.62.

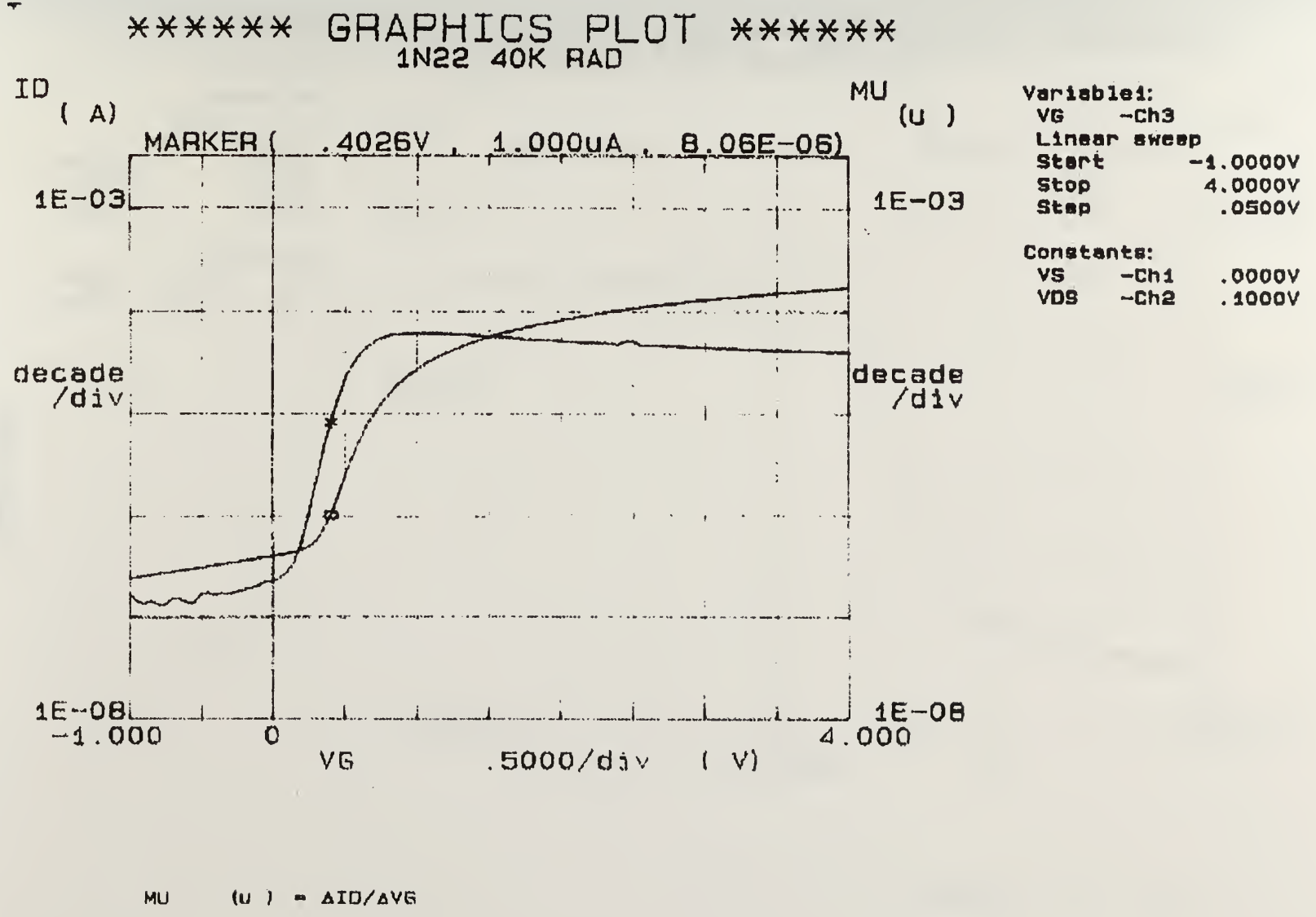
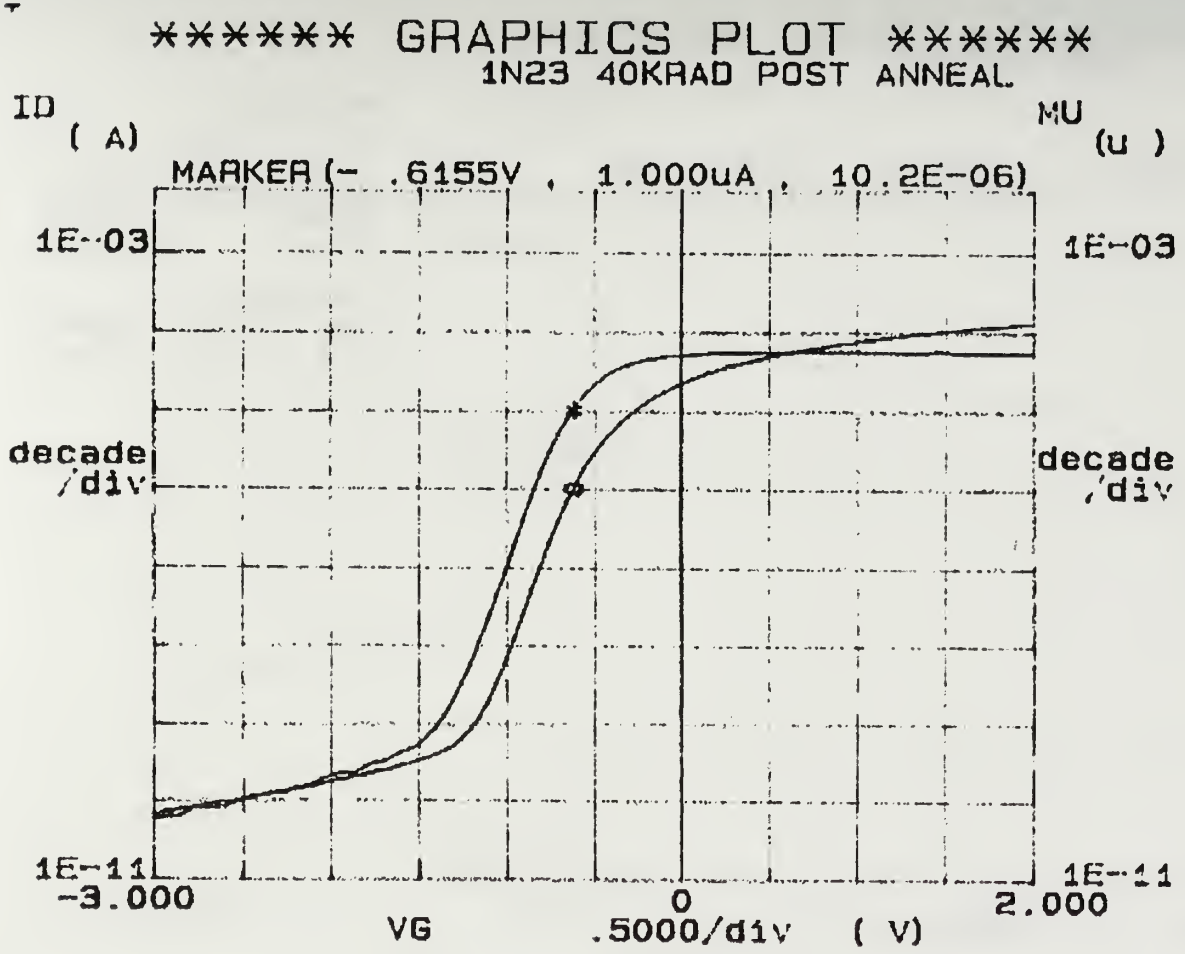

****** GRAPHICS PLOT ******
1N22 40K RAD
ID
(A)
MU
(u)
MARKER (.4026V , 1.000uA , 8.06E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-08
1E-08
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.63.



Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V

Constants:
VB -Ch1 .0000V
VDS -Ch2 .1000V

Figure C.64.

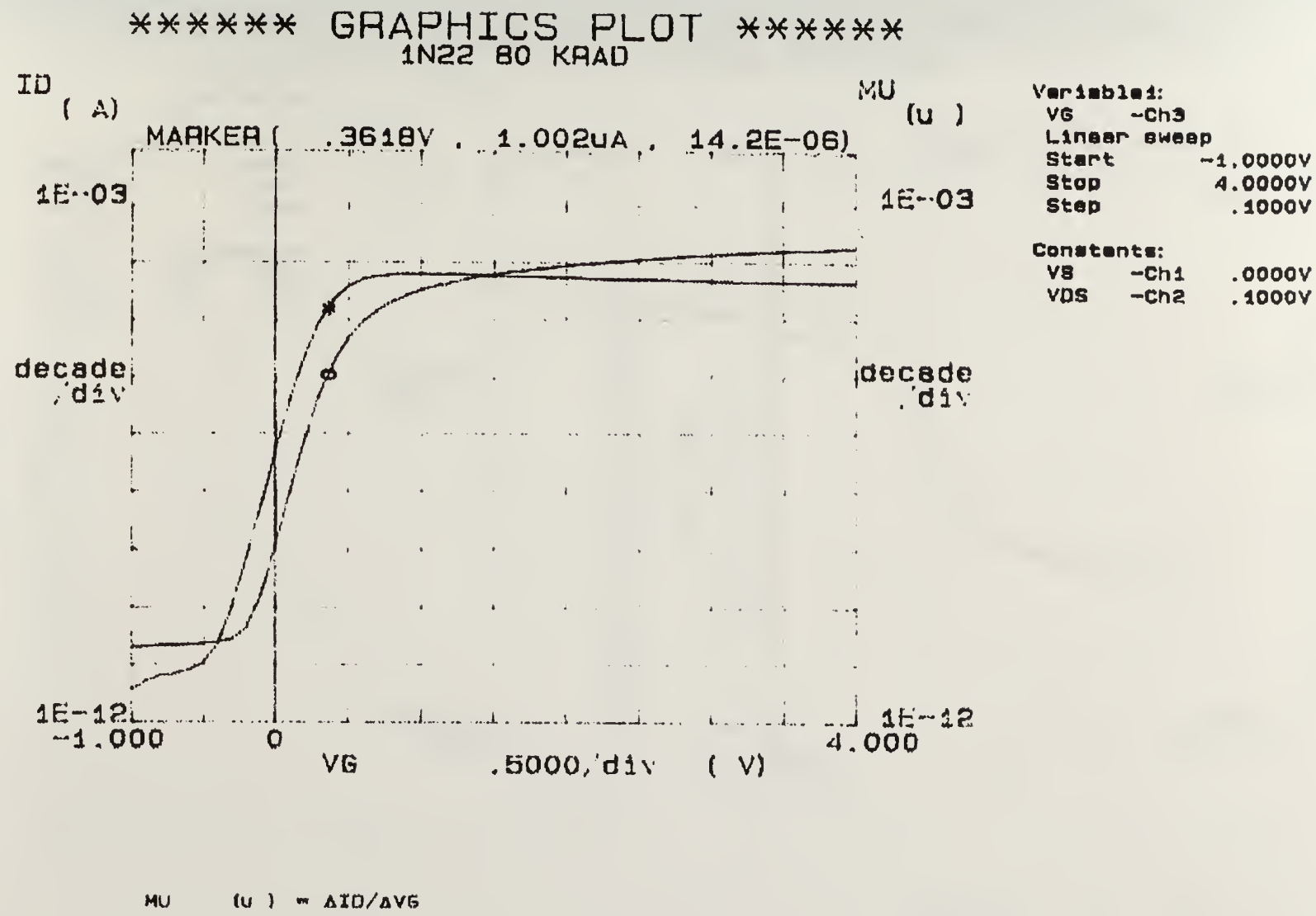

****** GRAPHICS PLOT ******
1N22 80 KRAD
ID
(A)
MARKER (.3618V , 1.002uA , 14.2E-06)
1E-03
decade
/div
1E-12
-1.000
0
VG
.5000/div
(V)
4.000
MU
(u)
1E-03
decade
/div
1E-12
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .1000V
Constants:
VB -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.65.

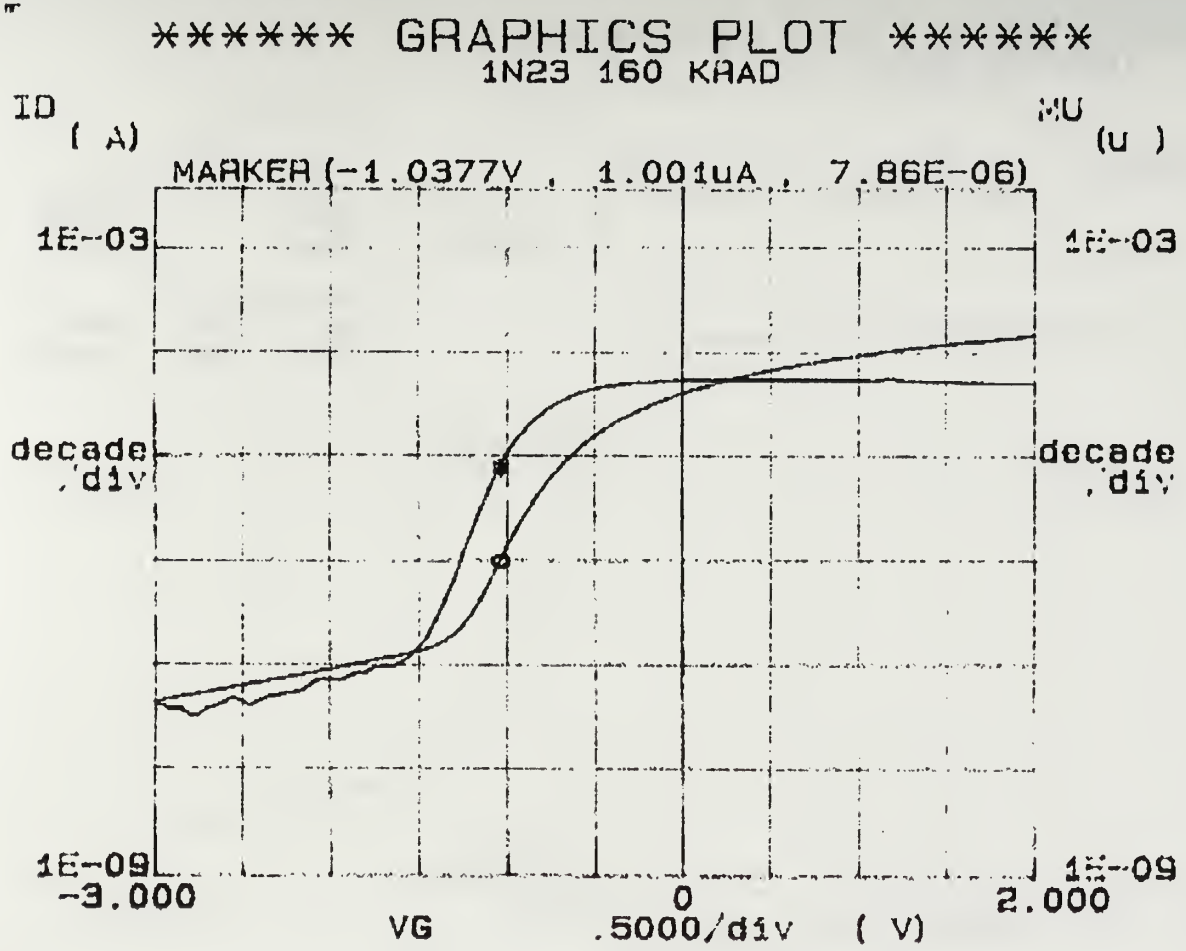

****** GRAPHICS PLOT ******
1N23 160 KRAD
ID
(A)
MU
(u)
MARKER(-1.0377V , 1.001uA , 7.86E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-09
1E-09
-3.000
0
2.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.66.

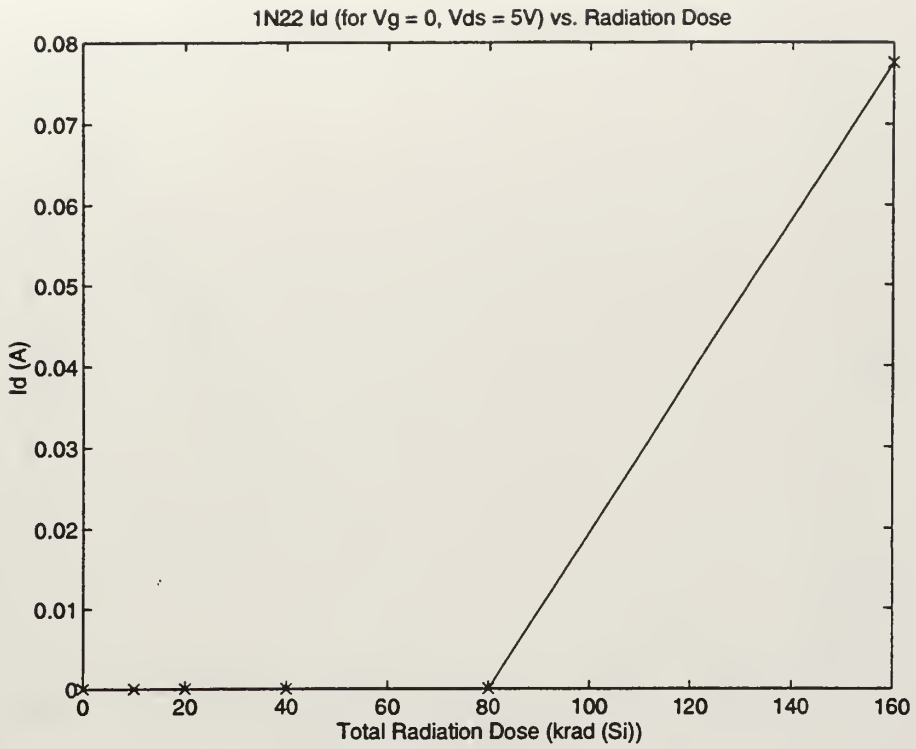


Figure C.67.

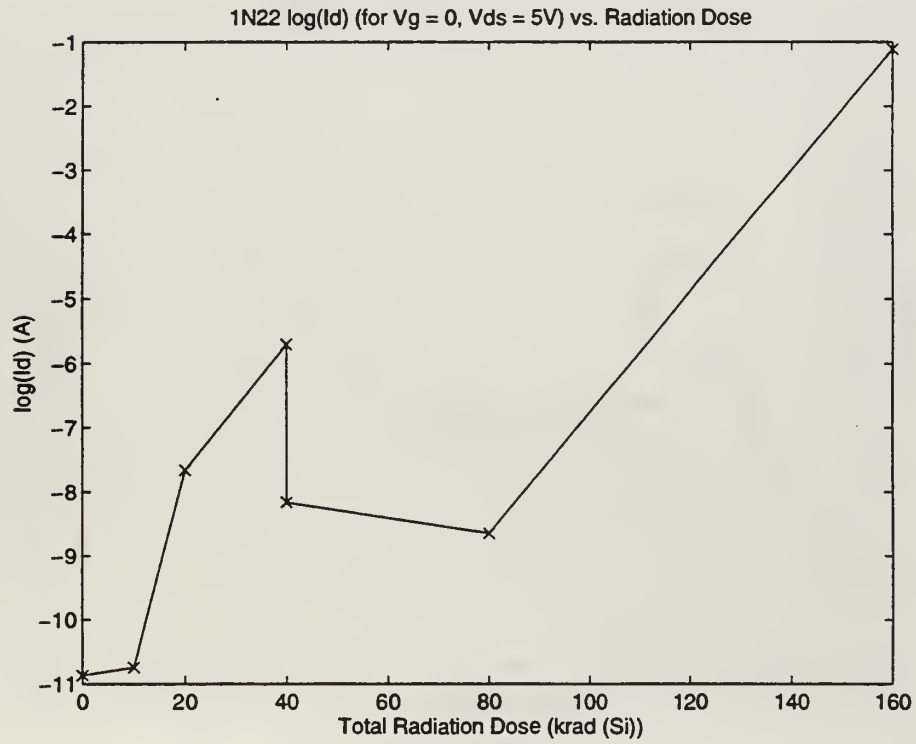


Figure C.68.

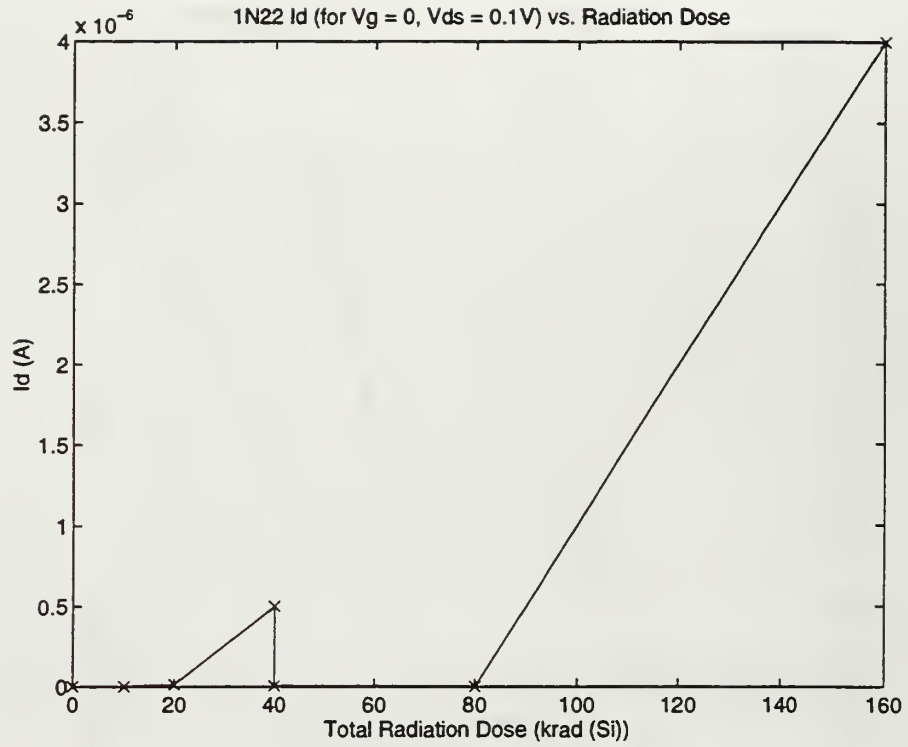


Figure C.69.

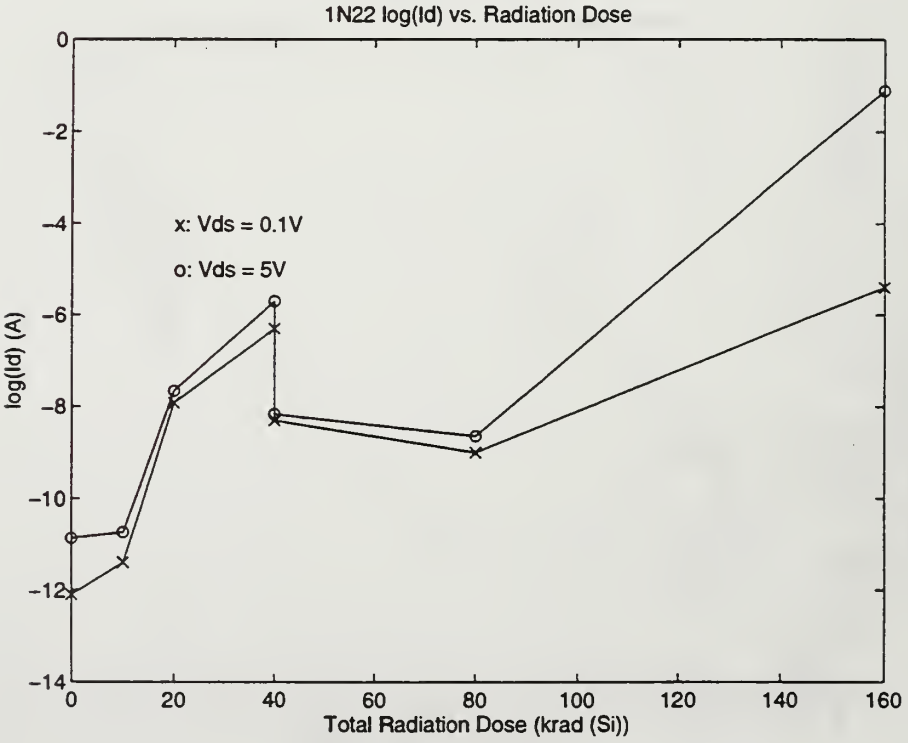


Figure C.70.

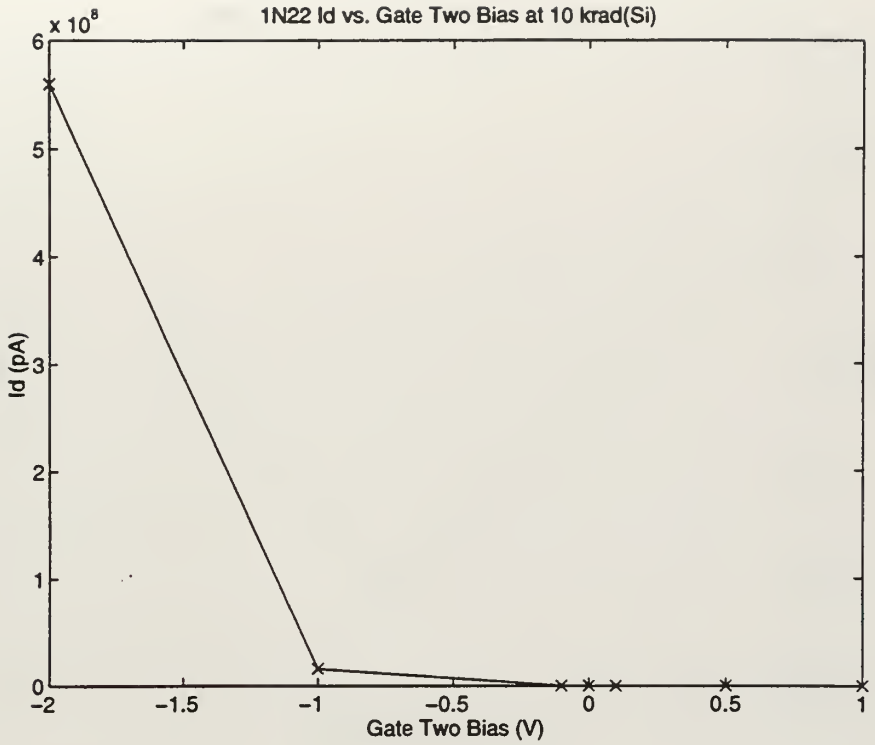


Figure C.71.

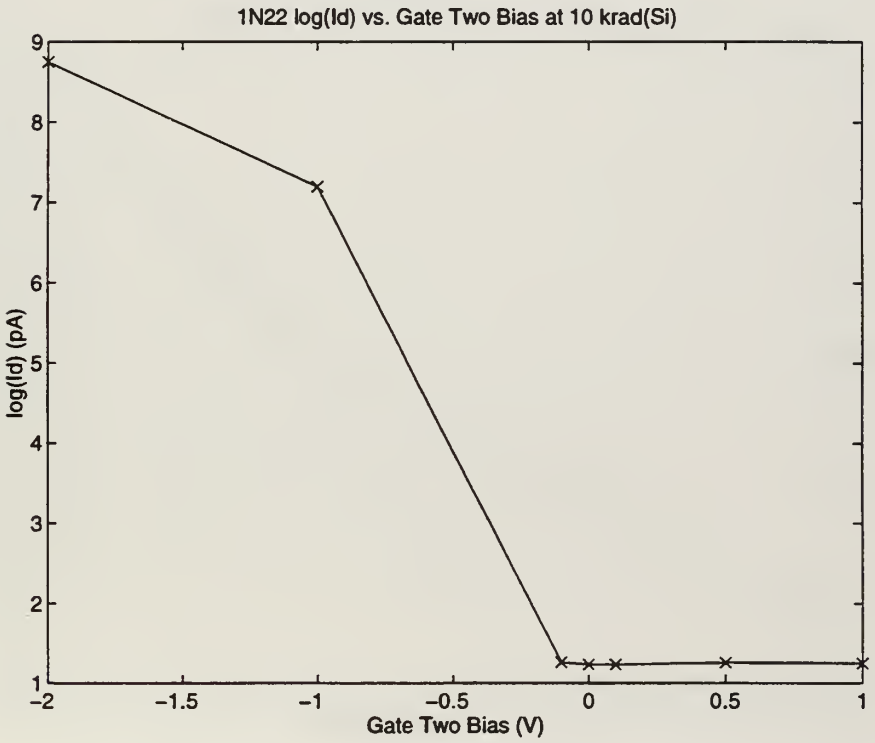


Figure C.72.

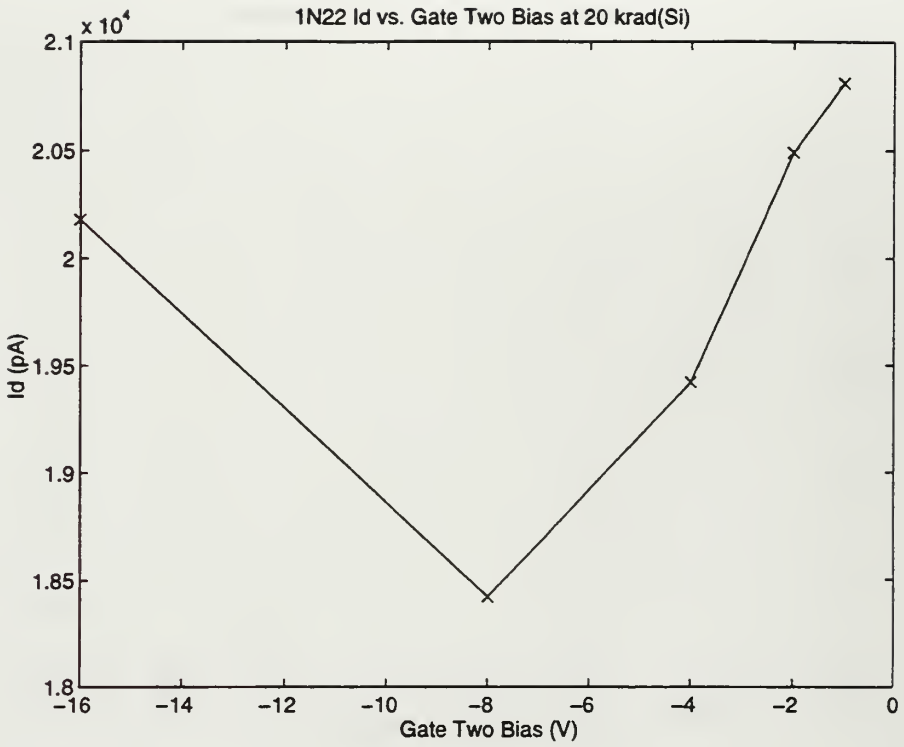


Figure C.73.

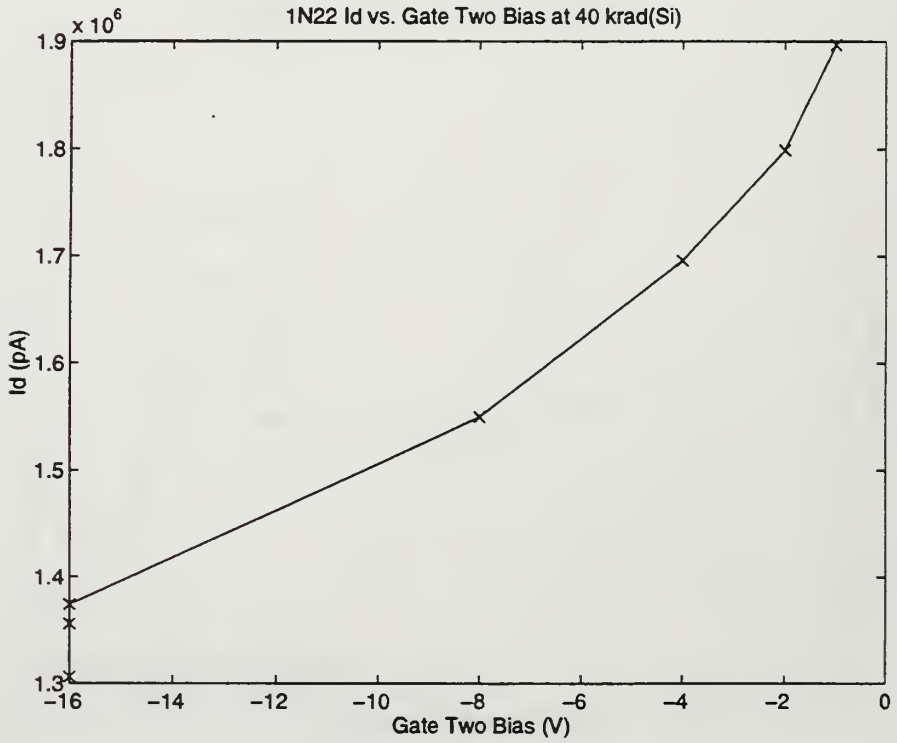


Figure C.74.

Figure C.75.

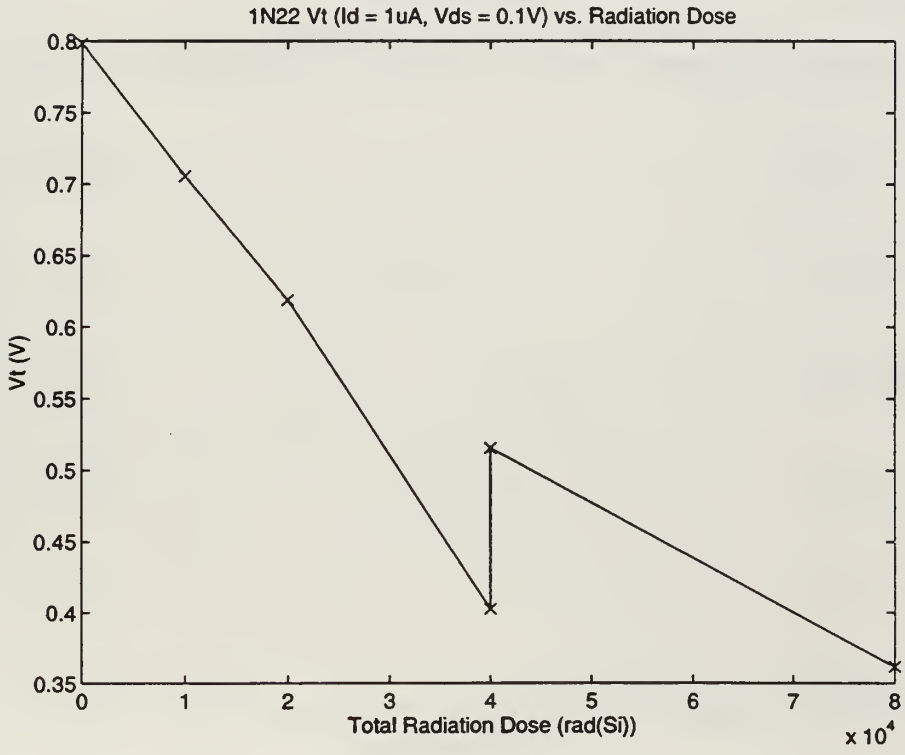


Figure C.76.

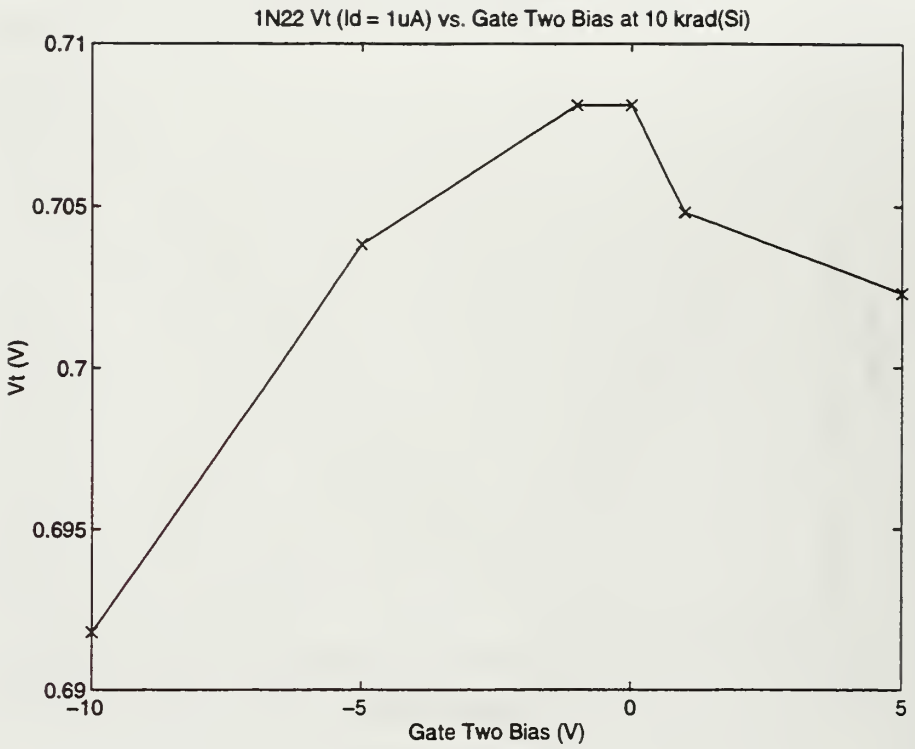


Figure C.77.

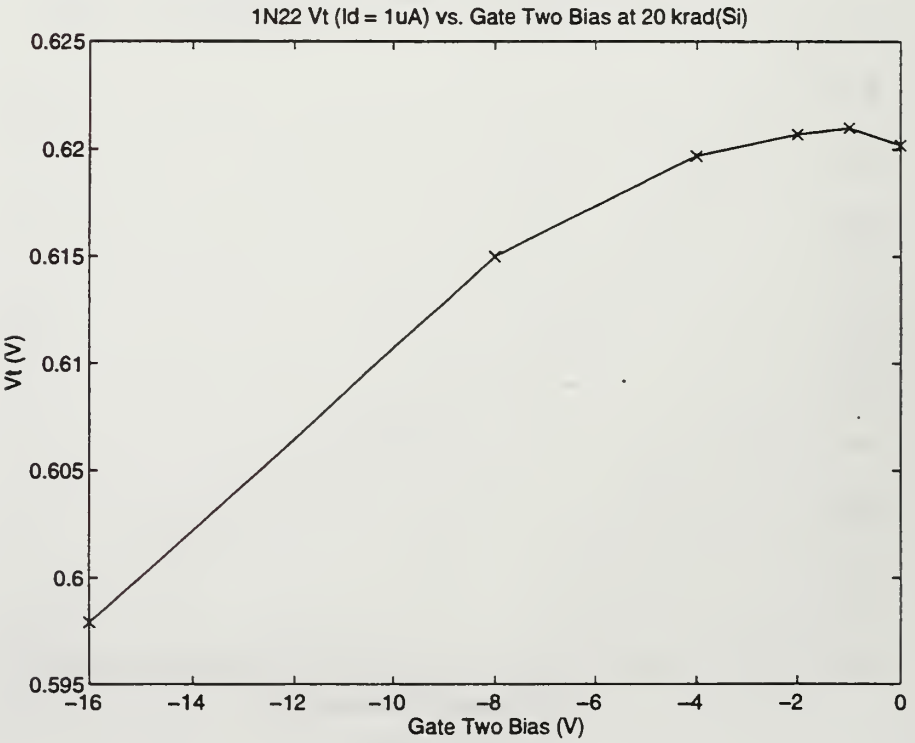


Figure C.78.

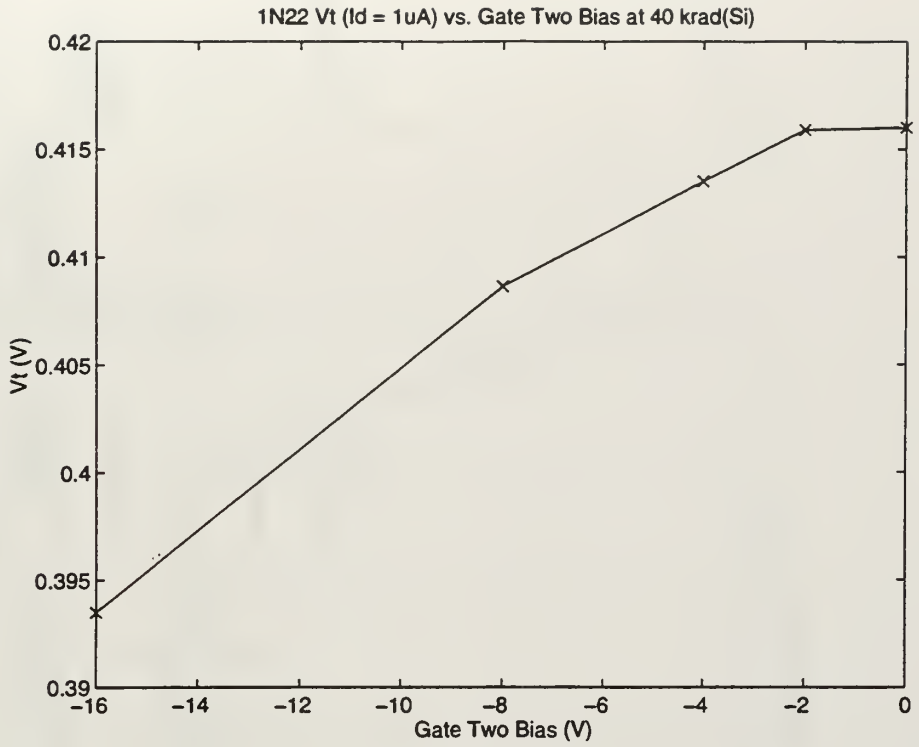


Figure C.79.

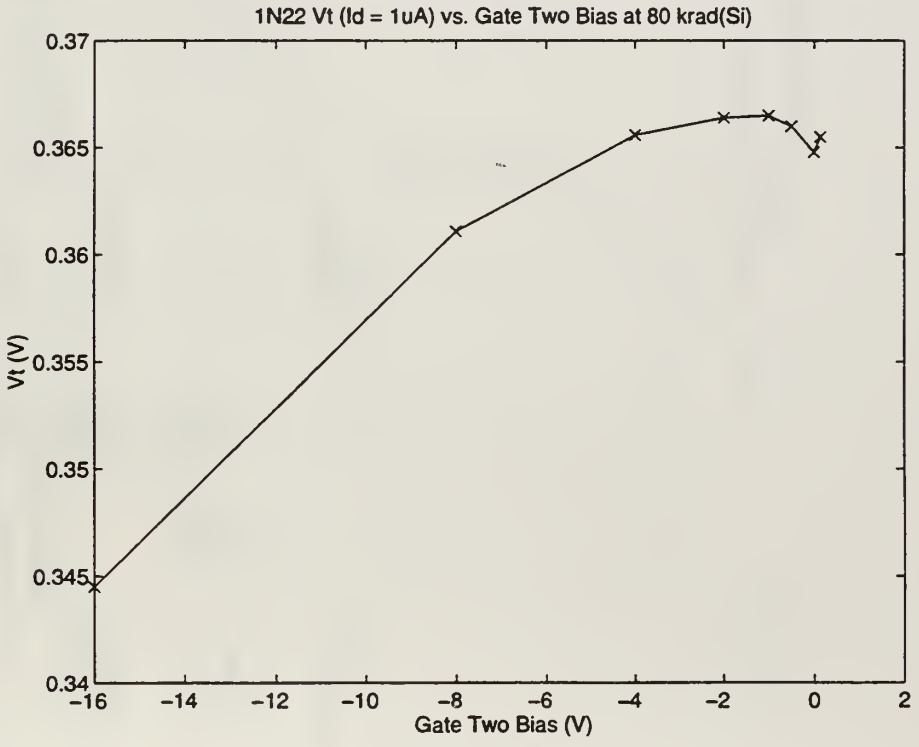


Figure C.80.

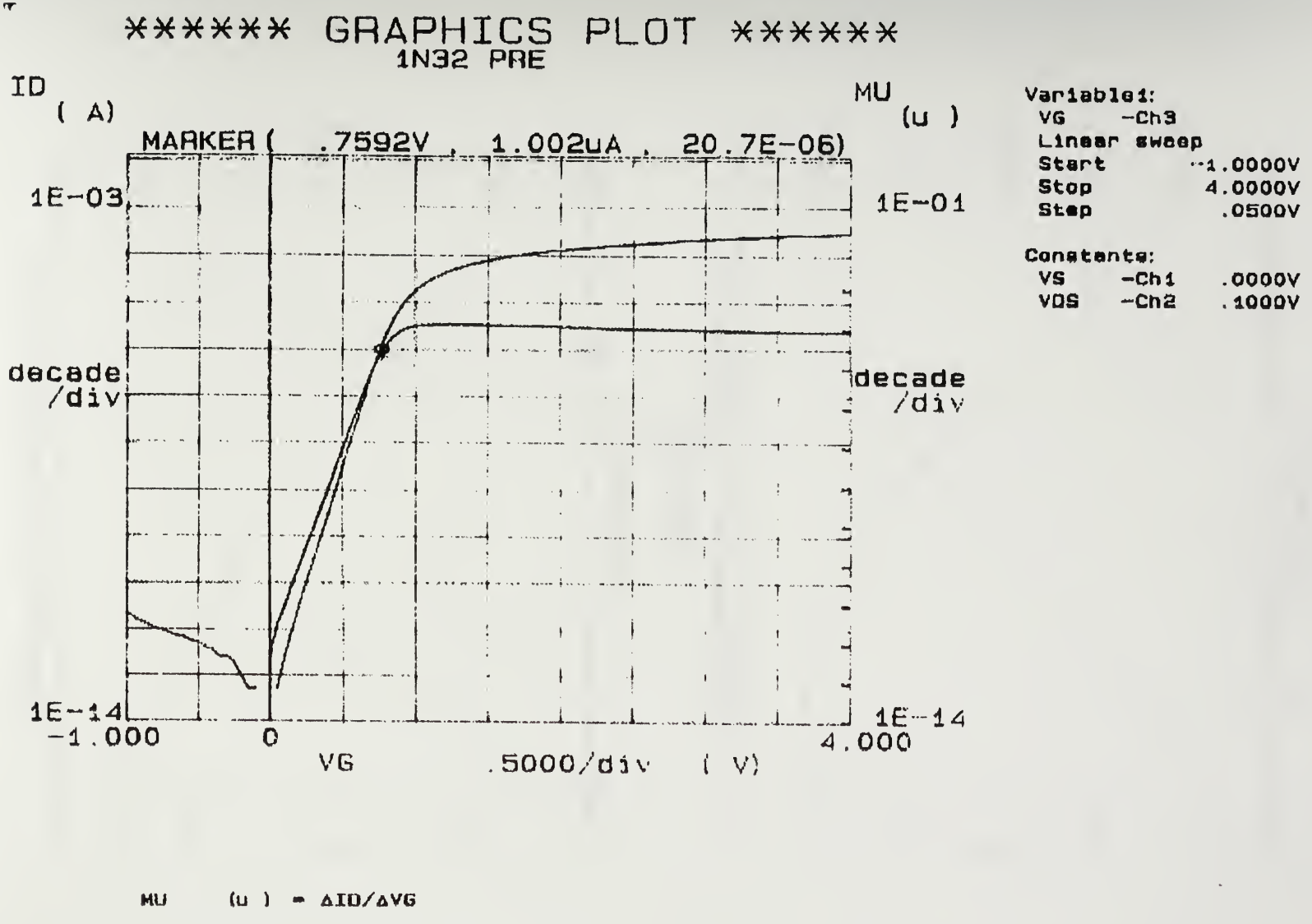

****** GRAPHICS PLOT ******
1N32 PRE
ID
(A)
MU
(u)
MARKER (.7592V , 1.002uA , 20.7E-06)
1E-03
1E-01
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.81.

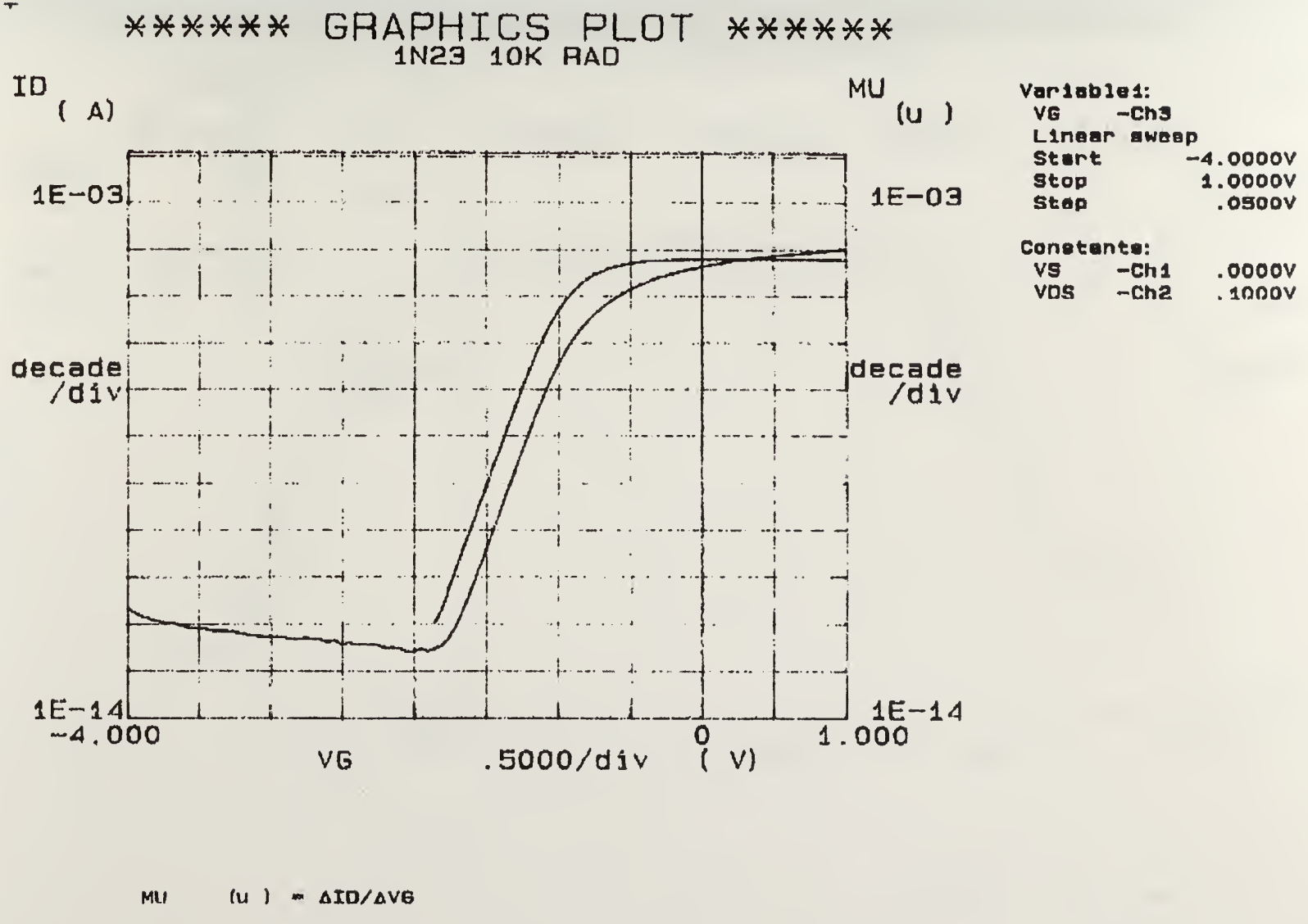

****** GRAPHICS PLOT ******
1N23 10K RAD
ID
(A)
MU
(u)
1E-03
1E-03
decade
/div
decade
/div
1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -4.0000V
Stop 1.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.82.

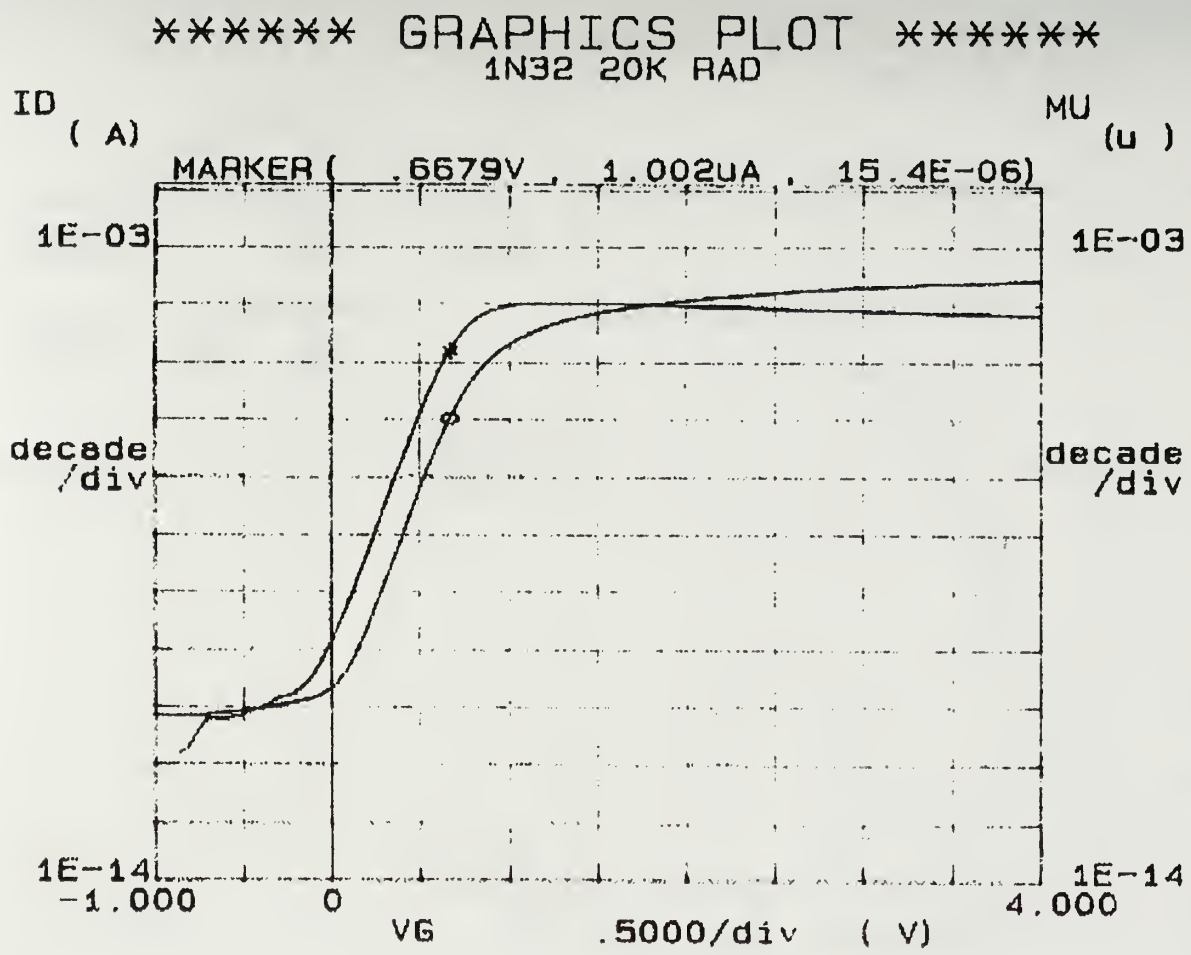

****** GRAPHICS PLOT ******
1N32 20K RAD
ID
(A)
MU
(u)
MARKER (.6679V , 1.002uA , 15.4E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.83.

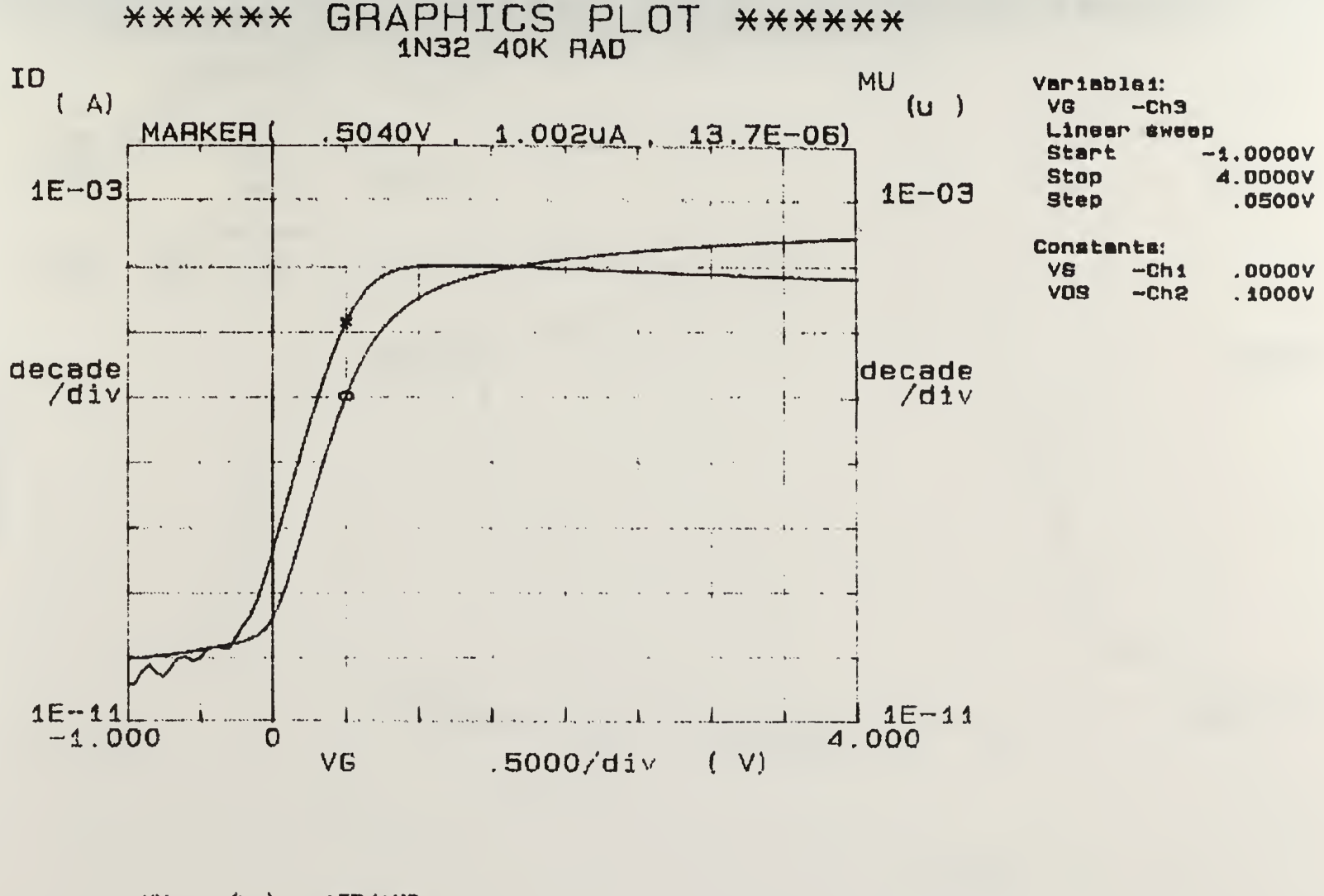

****** GRAPHICS PLOT ******
1N32 40K RAD
ID
(A)
MU
(u)
MARKER (.5040V , 1.002uA , 13.7E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-11
1E-11
-1.000
0
4.000
VG .5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = AID/AVG

Figure C.84.

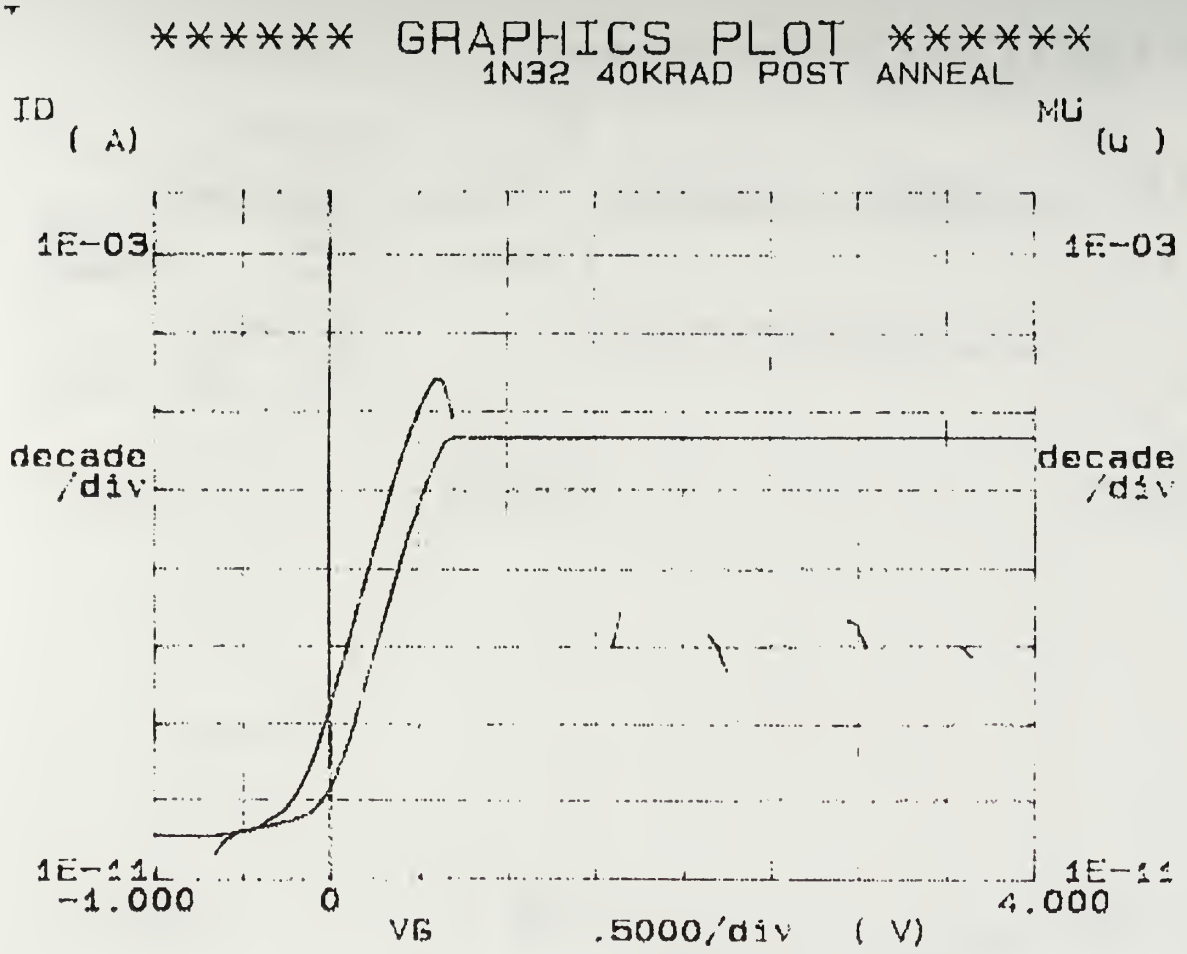

****** GRAPHICS PLOT ******
1N32 40KRAD POST ANNEAL
ID
(A)
MU
(u)
1E-03
1E-03
decade
/div
decade
/div
1E-11
1E-11
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.85.

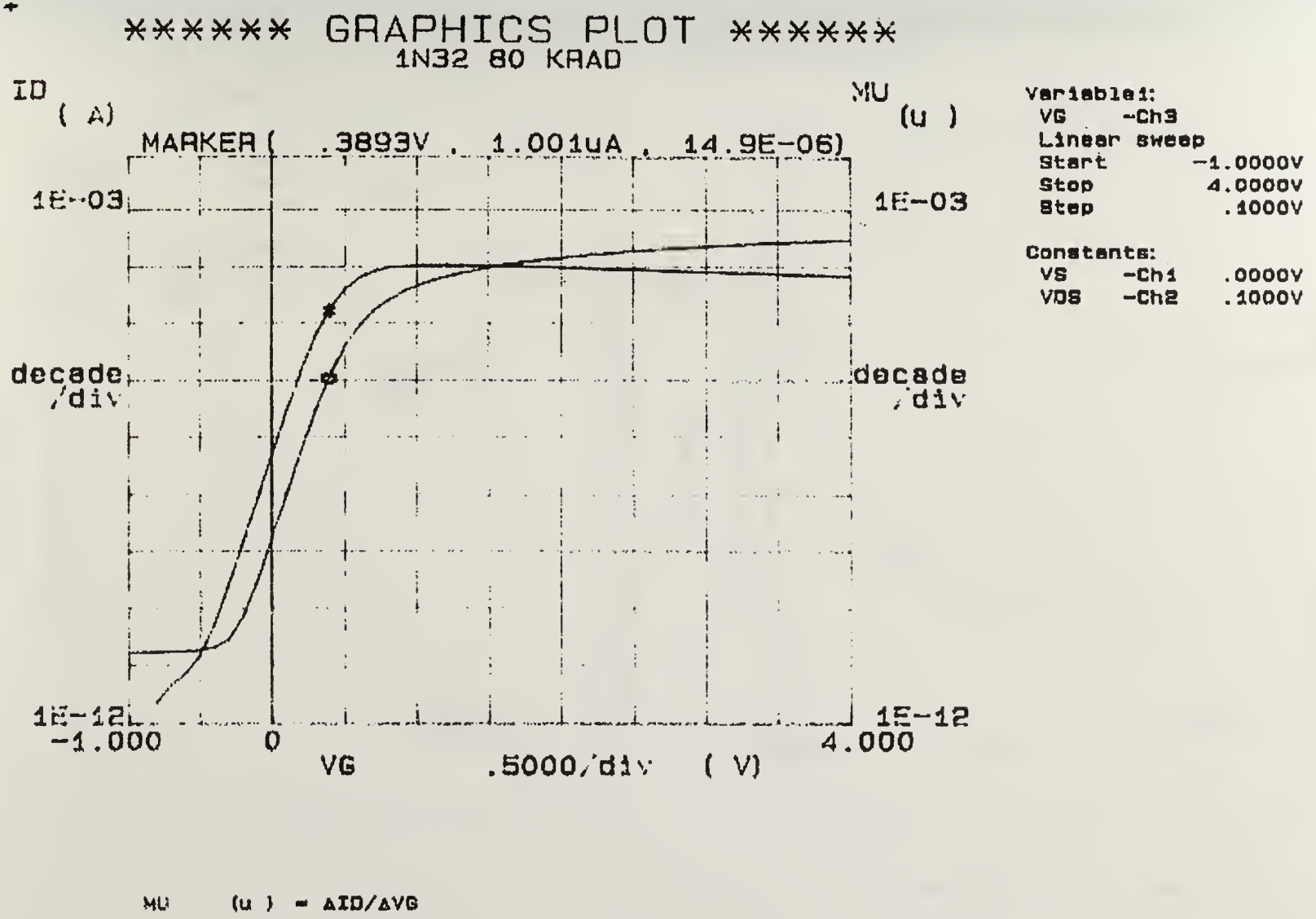

****** GRAPHICS PLOT ******
1N32 80 KRAD
ID
(A)
MU
(u)
MARKER(.3893V , 1.001uA , 14.9E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-12
1E-12
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .1000V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.86.

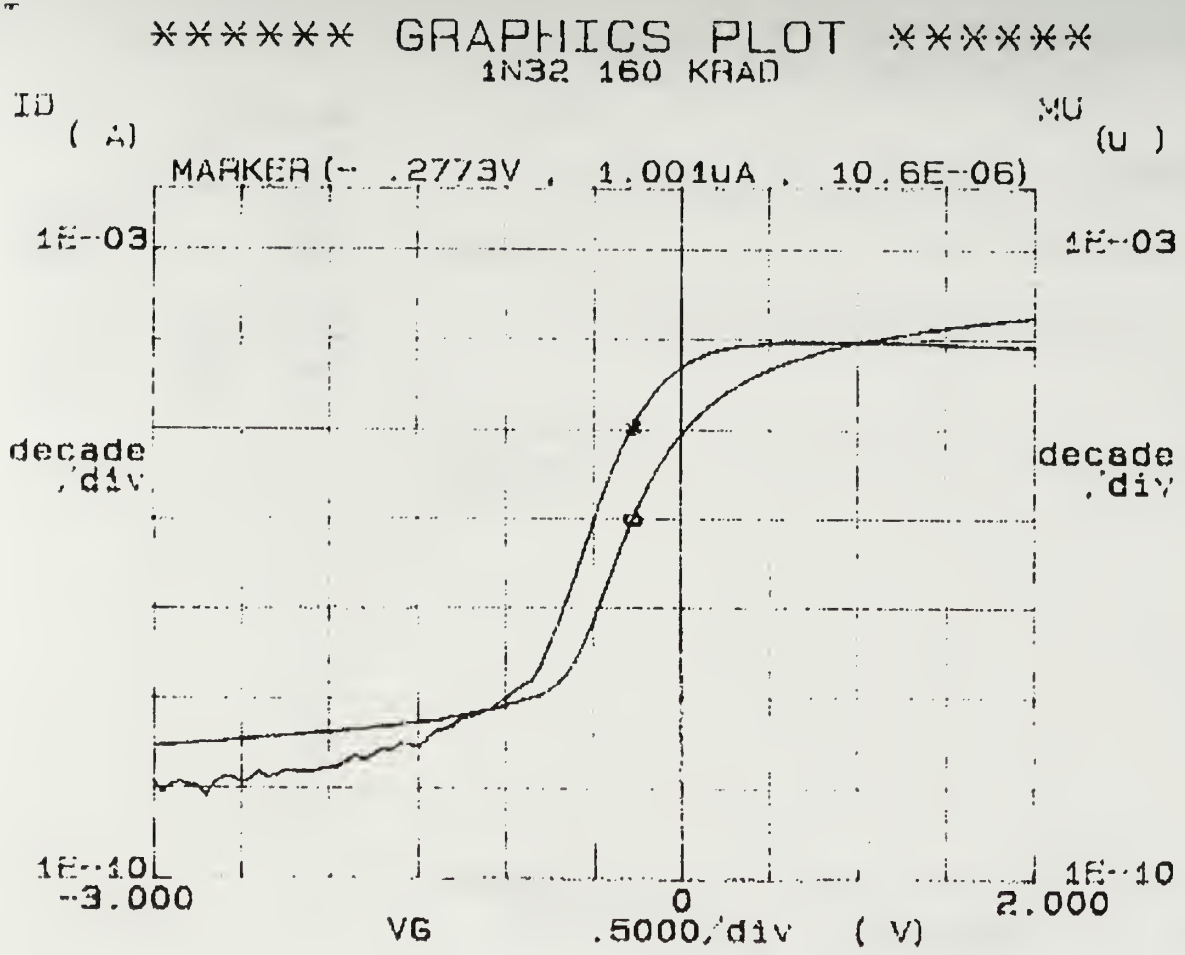

****** GRAPHICS PLOT ******
1N32 160 KRAD
ID
(A)
MU
(u)
MARKER (-.2773V , 1.001uA , 10.6E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-10
1E-10
-3.000
0
2.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.87.

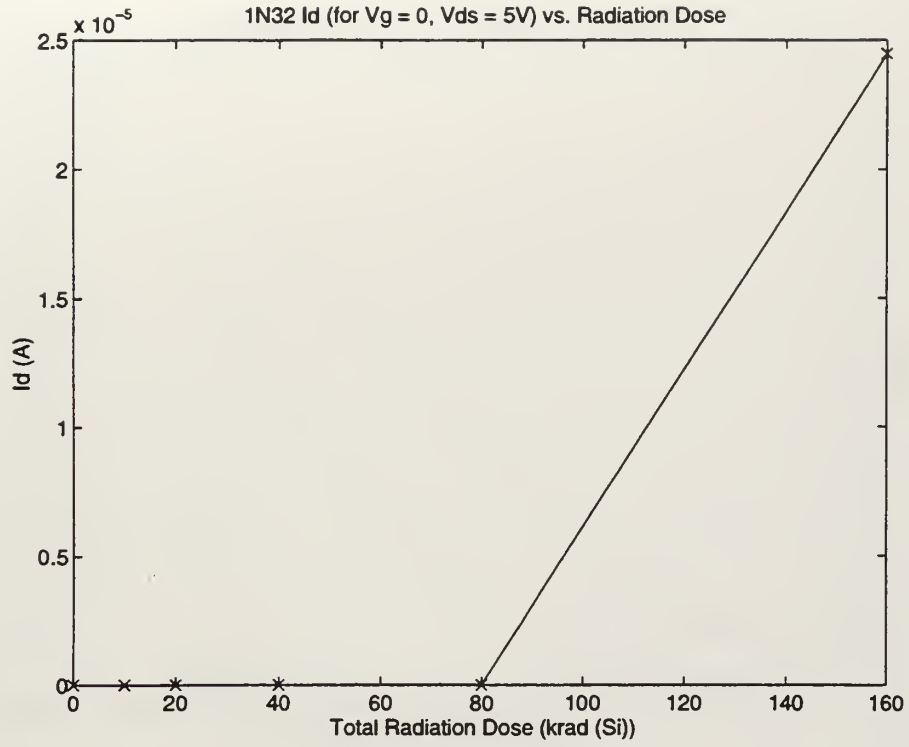


Figure C.88.

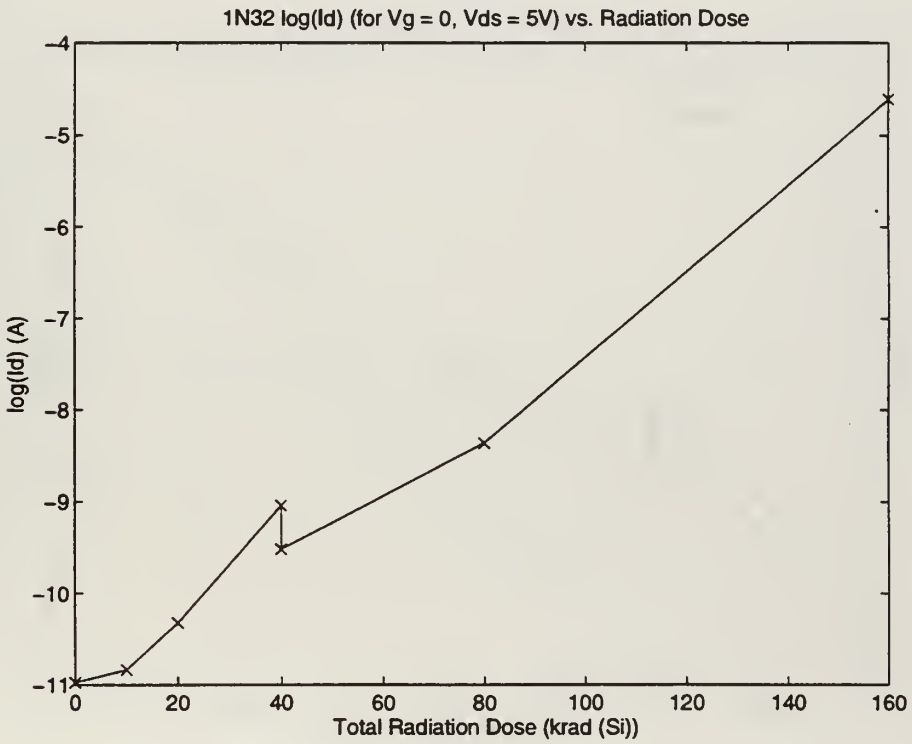


Figure C.89.

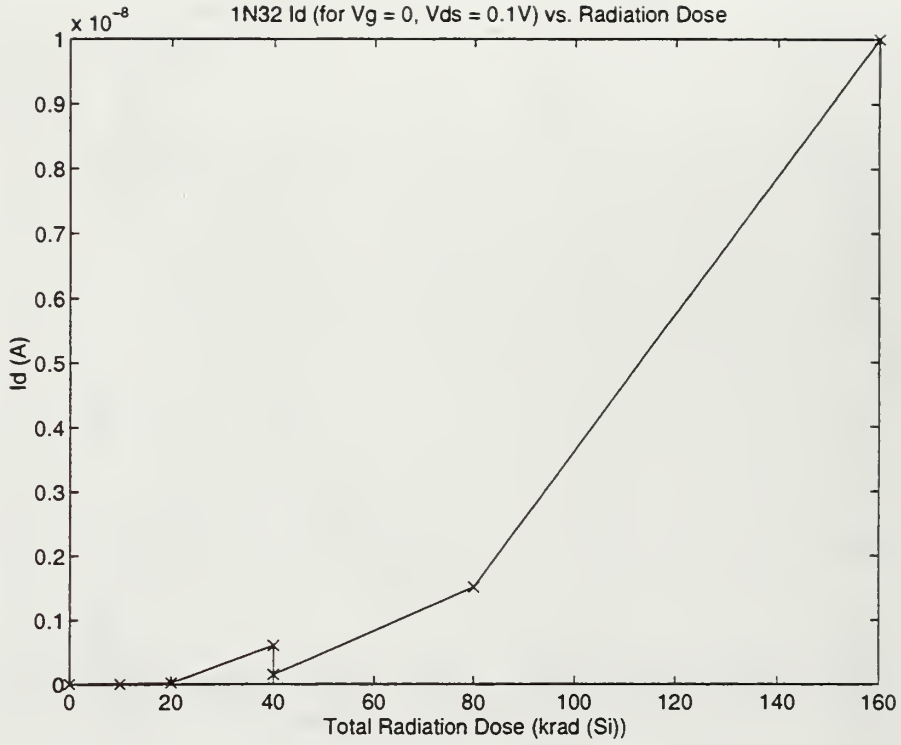


Figure C.90.

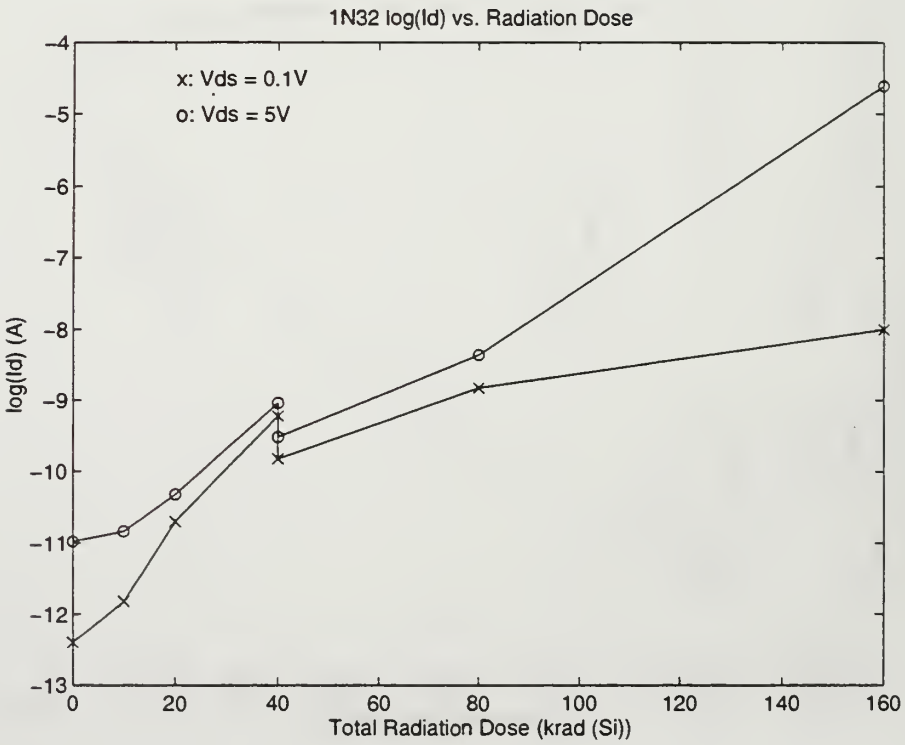


Figure C.91.

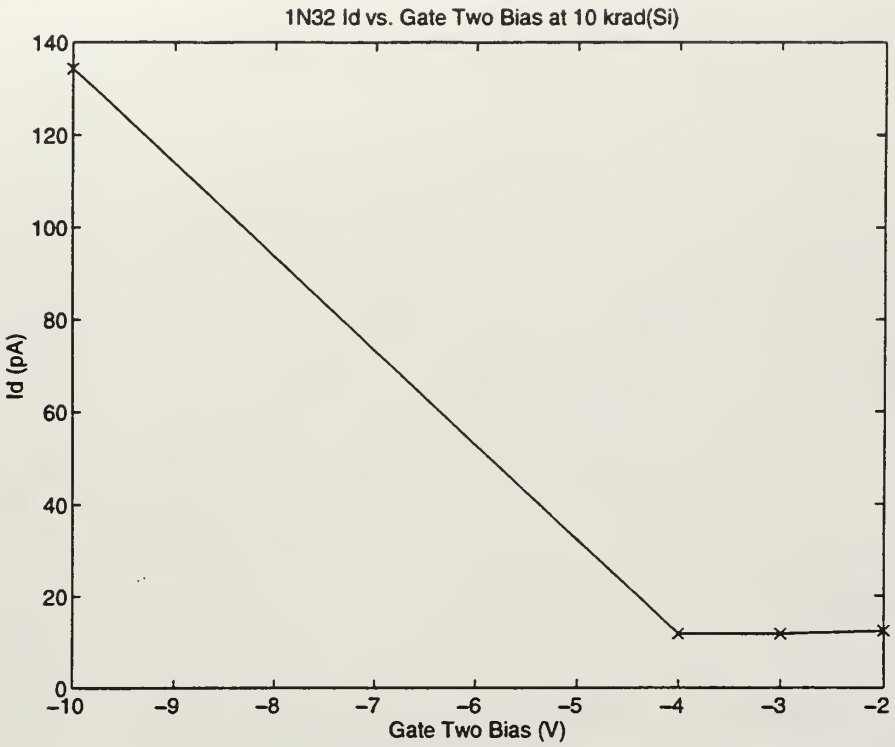


Figure C.92.

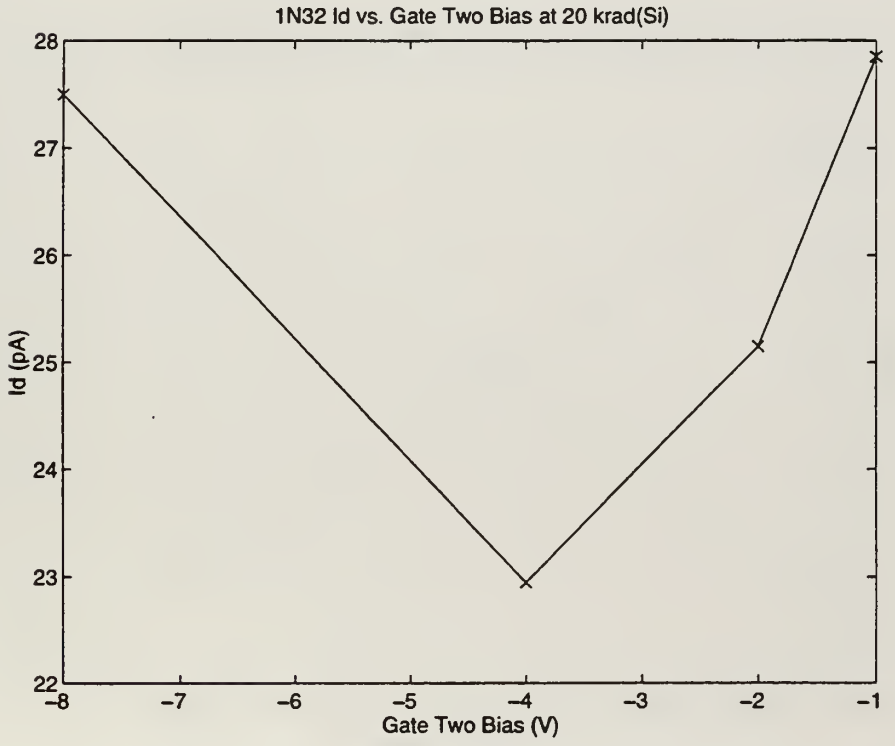


Figure C.93.

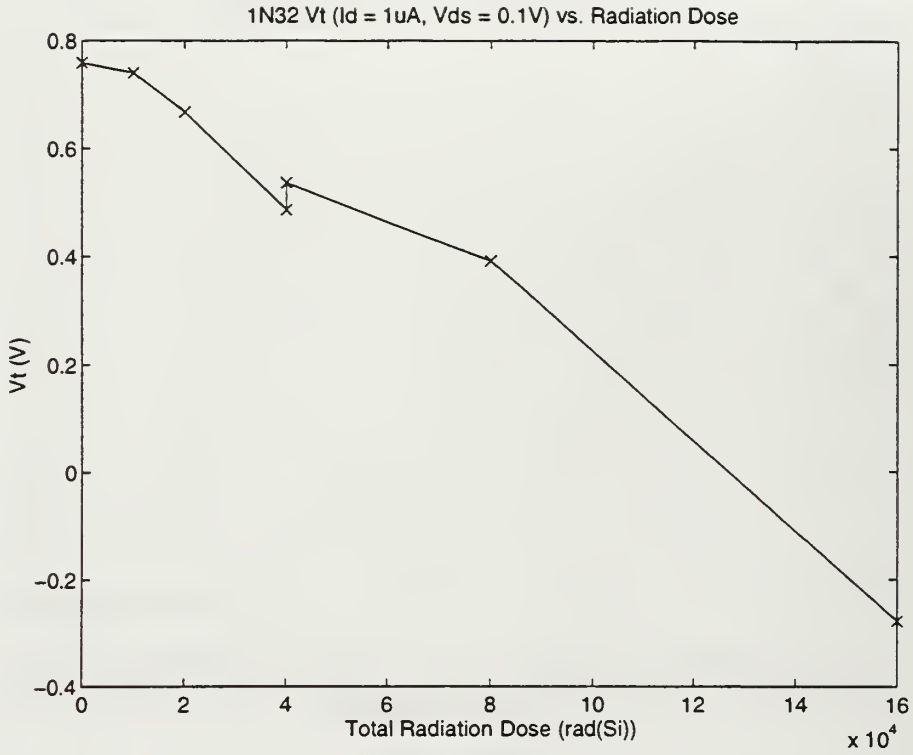


Figure C.94.

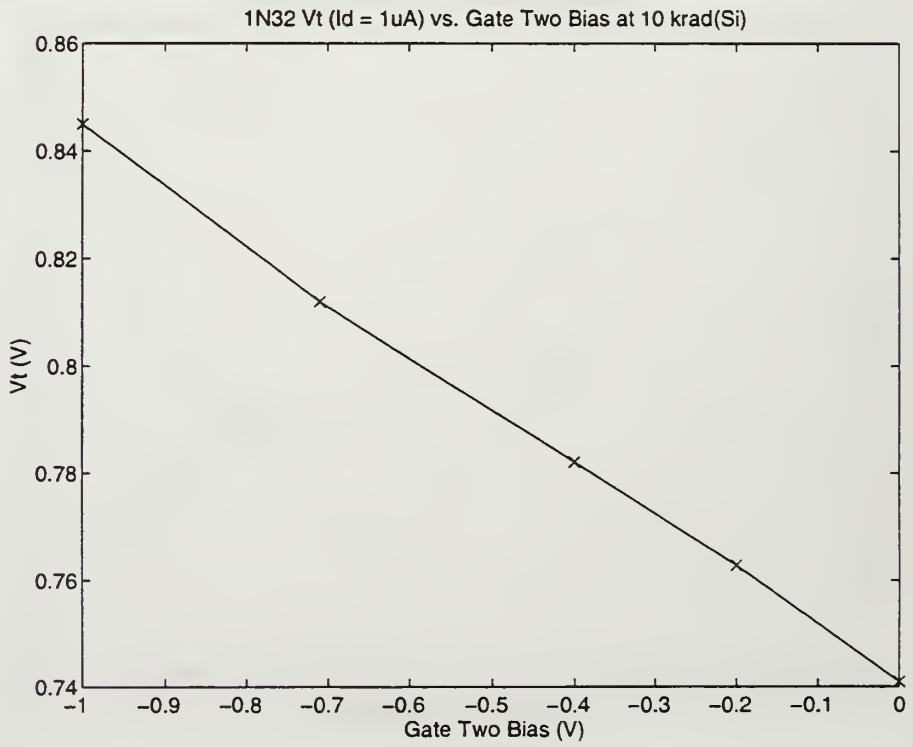


Figure C.95.

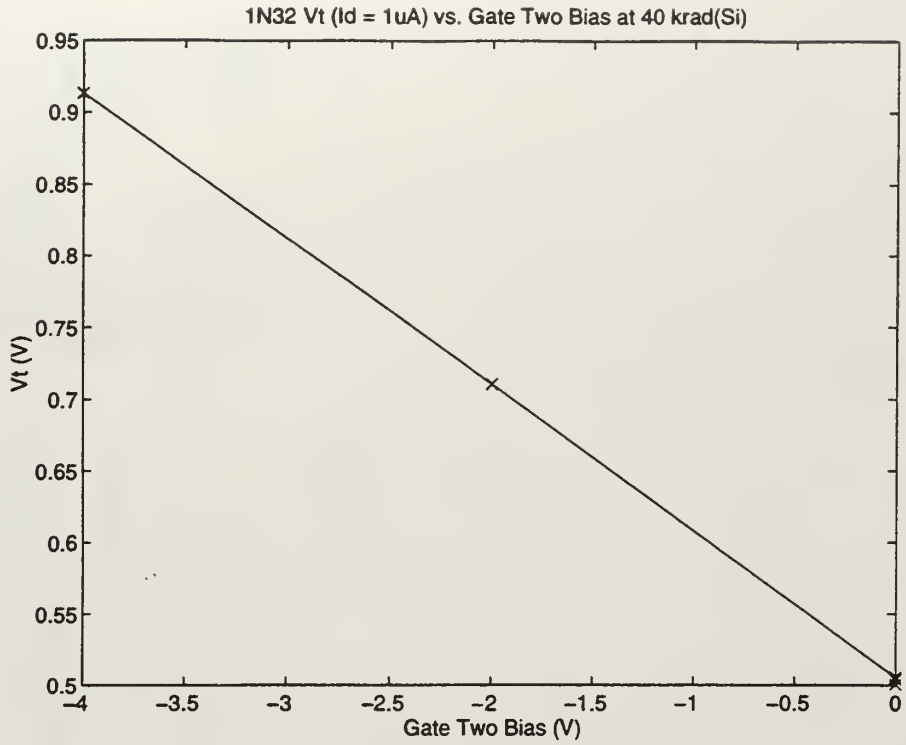


Figure C.96.

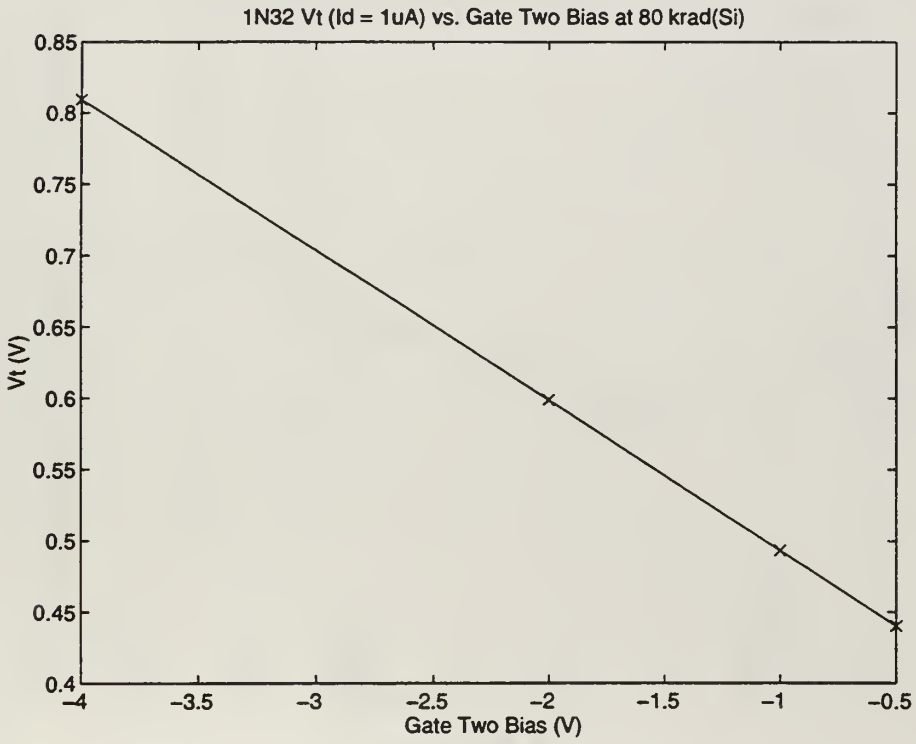


Figure C.97.

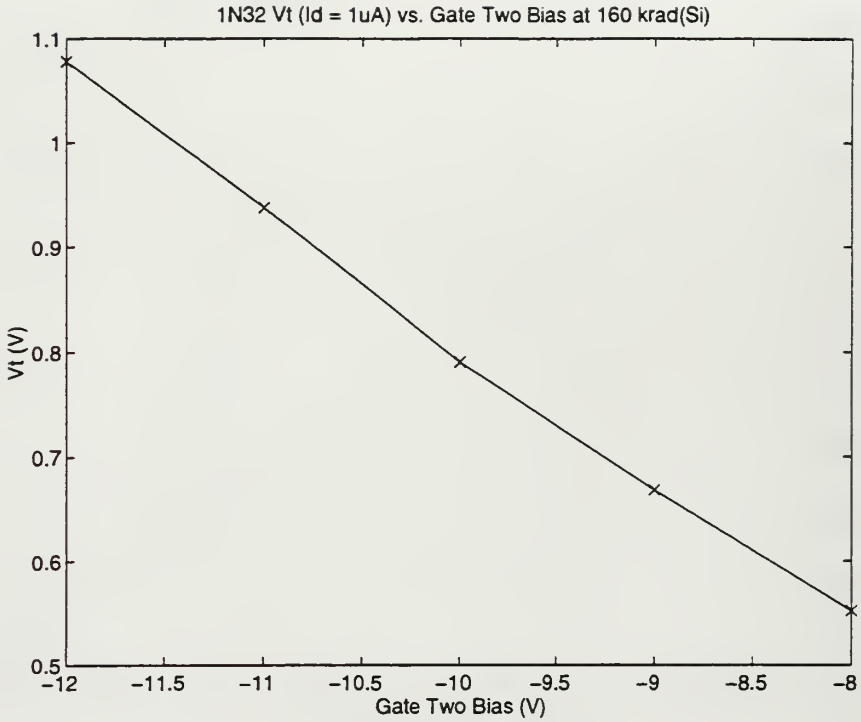


Figure C.98.

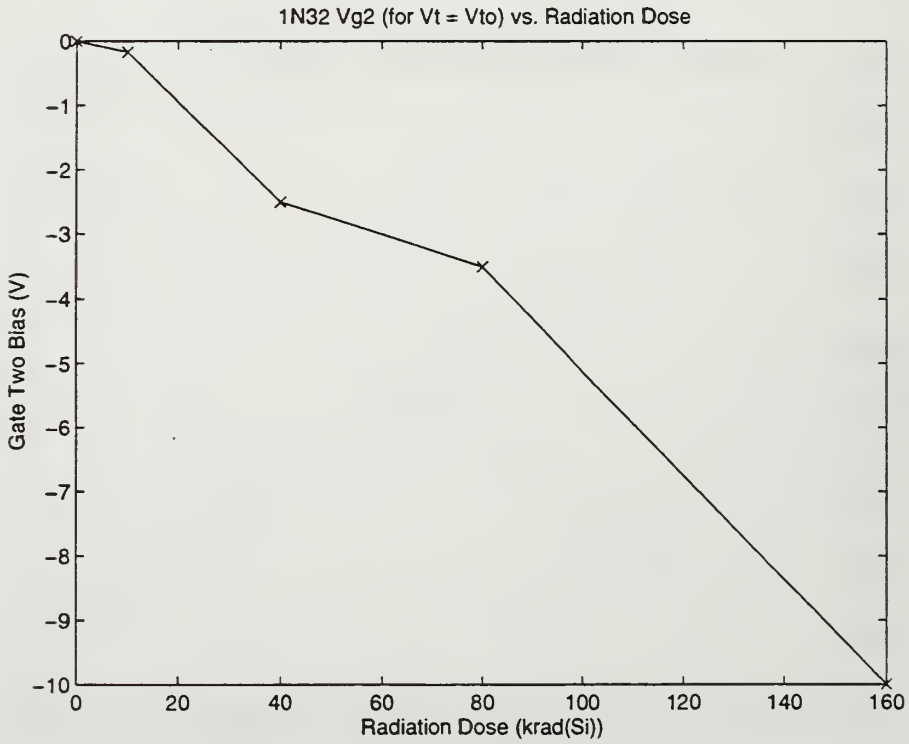


Figure C.99.

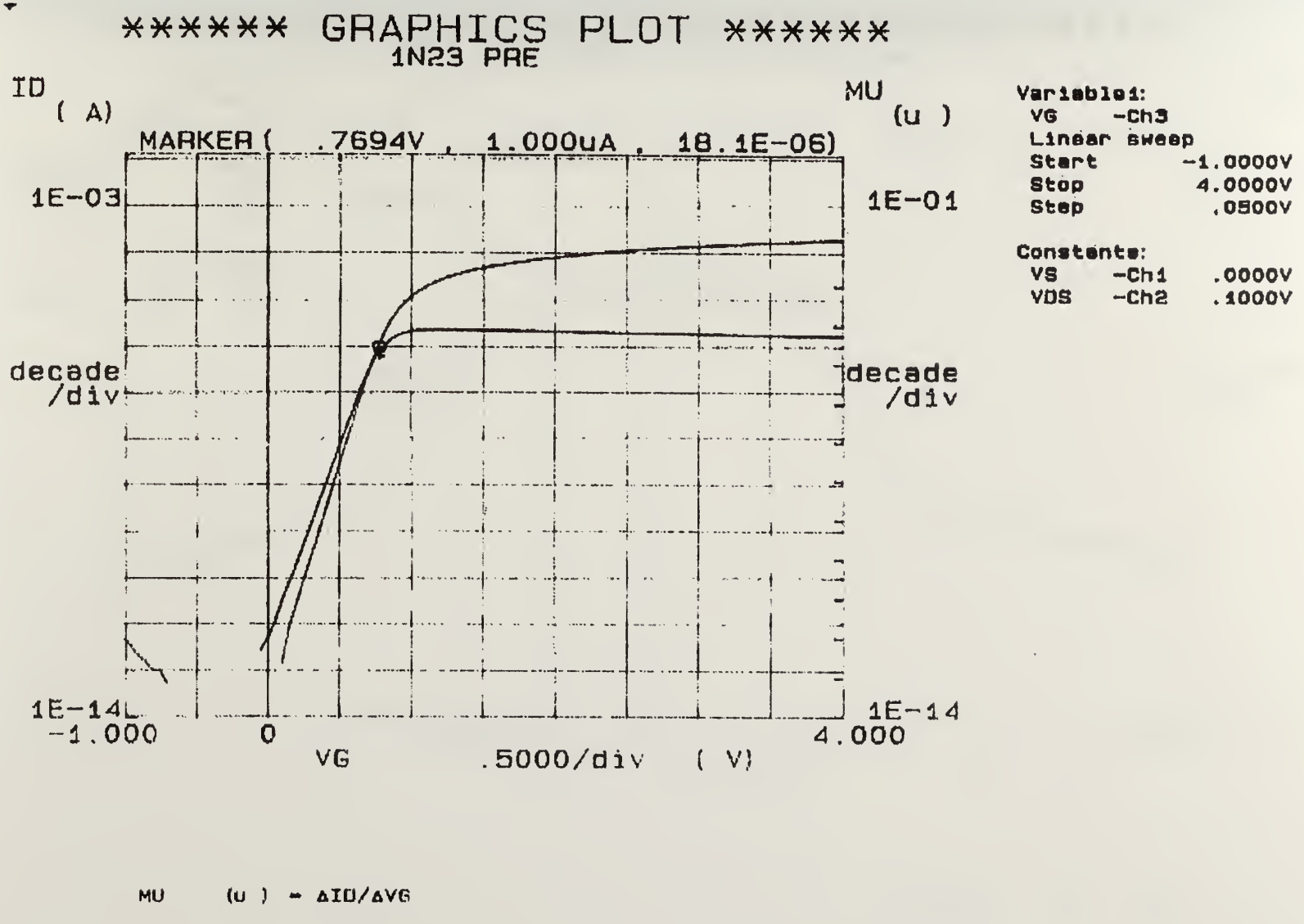

****** GRAPHICS PLOT ******
1N23 PRE
ID
(A)
MU
(u)
MARKER(.7694V , 1.000uA , 18.1E-06)
1E-03
1E-01
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.100.

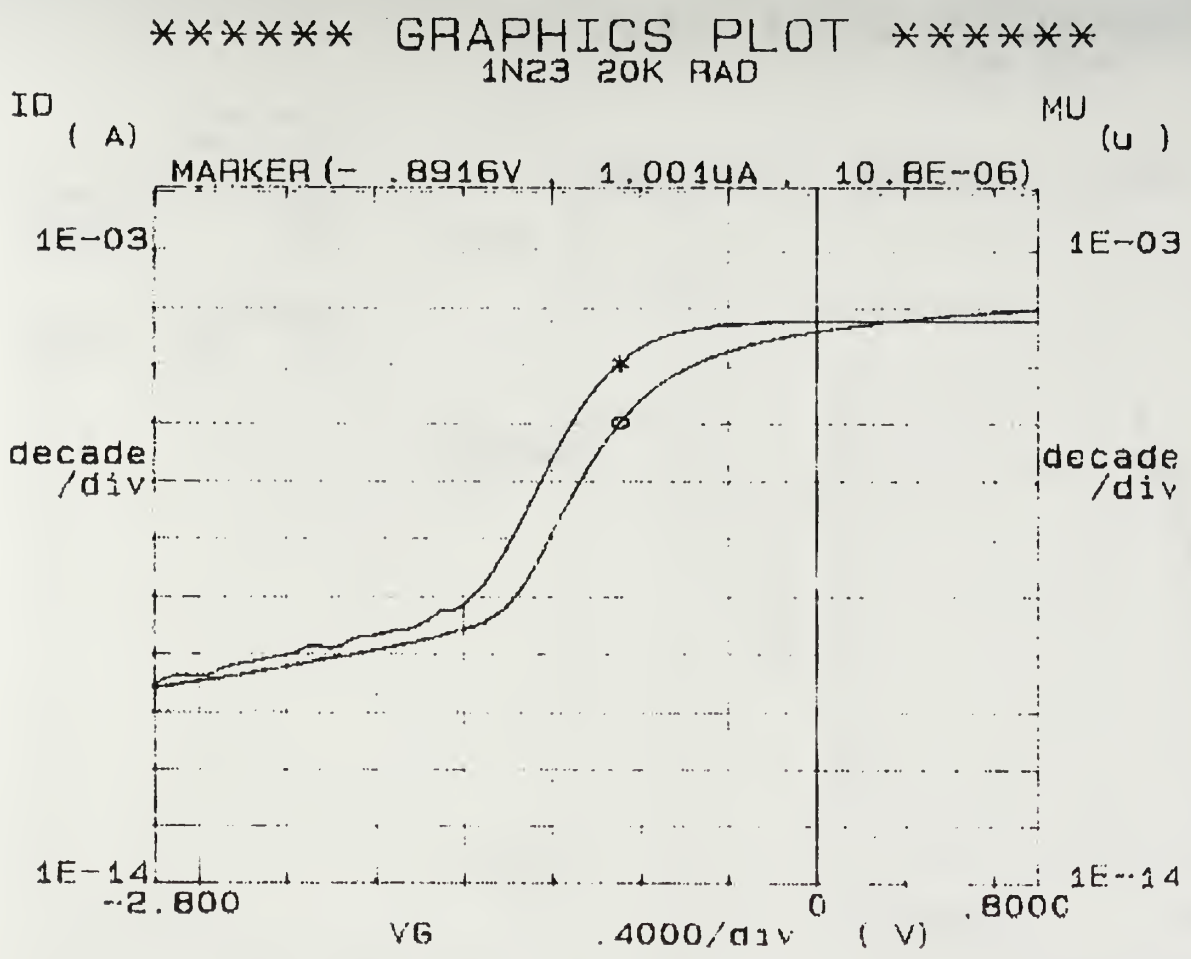

****** GRAPHICS PLOT ******
1N23 20K RAD
ID
(A)
MU
(u)
MARKER(- .8916V , 1.001uA , 10.8E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-14
1E-14
-2.800
0
.8000
VG
.4000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 1.0000V
Step .0500V
Constants:
VG -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.101.

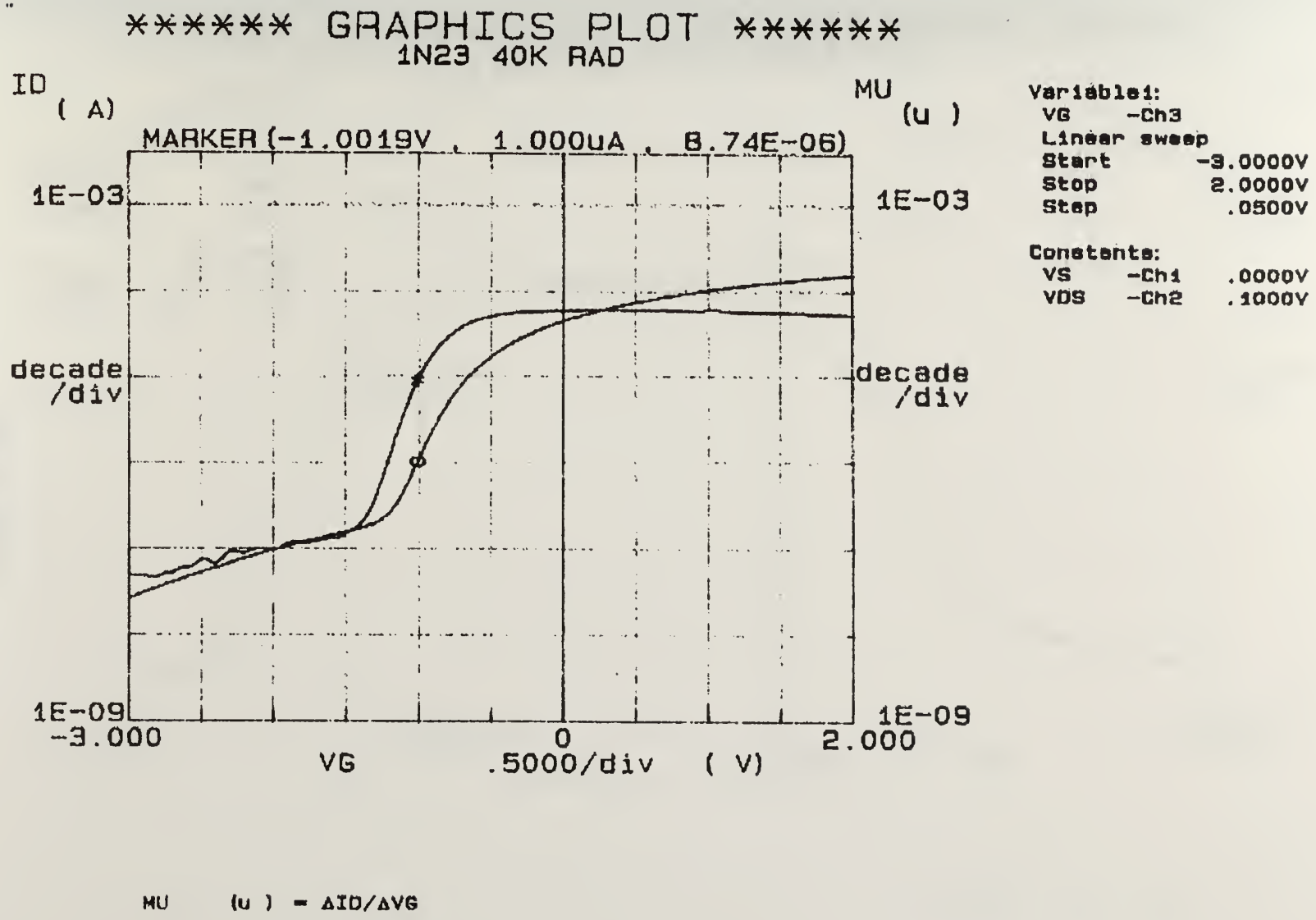

****** GRAPHICS PLOT ******
1N23 40K RAD
ID
(A)
MU
(u)
MARKER (-1.0019V , 1.000uA , 8.74E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-09
1E-09
-3.000
0
2.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.102.

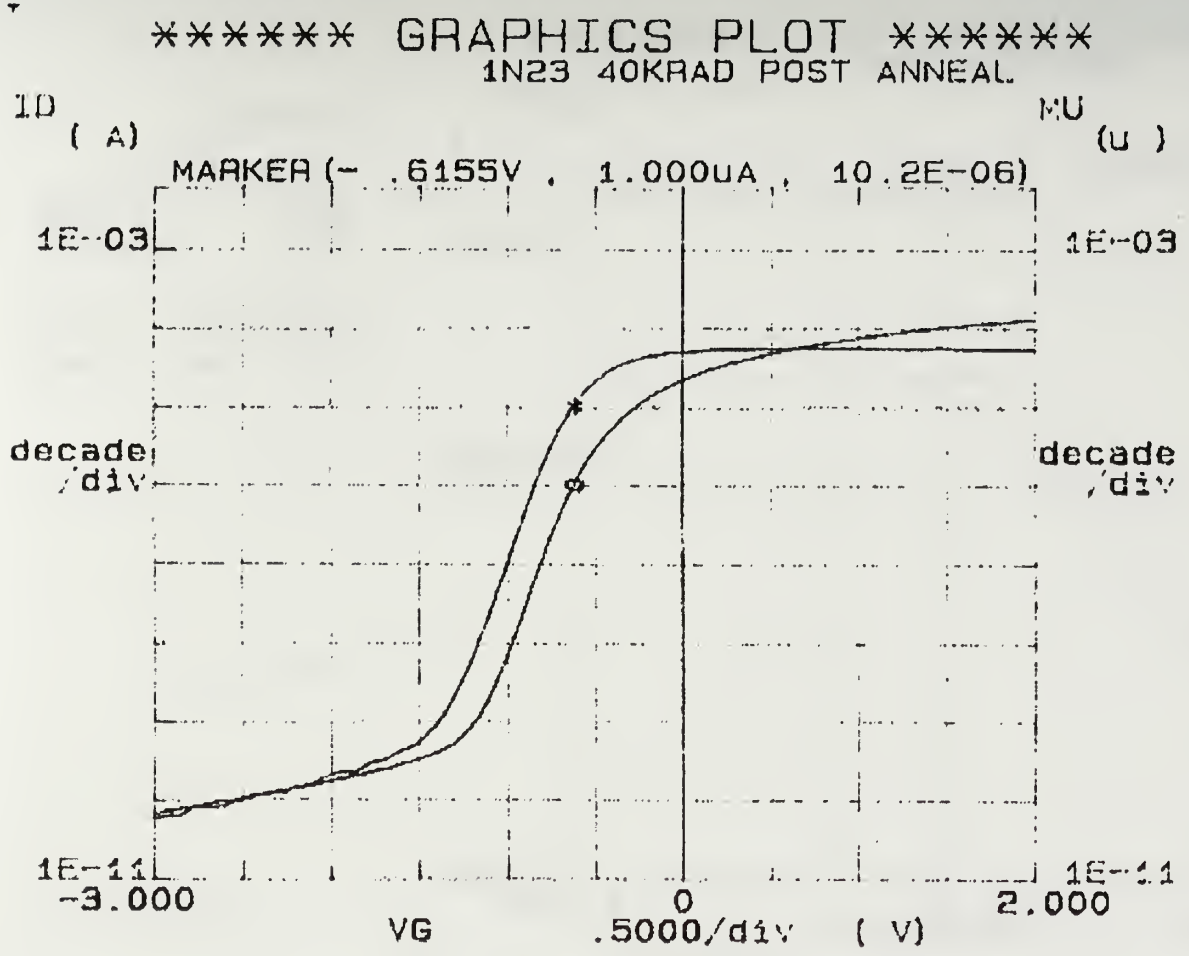

****** GRAPHICS PLOT ******
1N23 40KRAD POST ANNEAL
ID
(A)
MU
(u)
MARKER (- .6155V , 1.000uA , 10.2E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-11
1E-11
-3.000
0
2.000
VG
.5000/div
(V)
MU (u) = ΔID/ΔVG
Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V

Figure C.103.

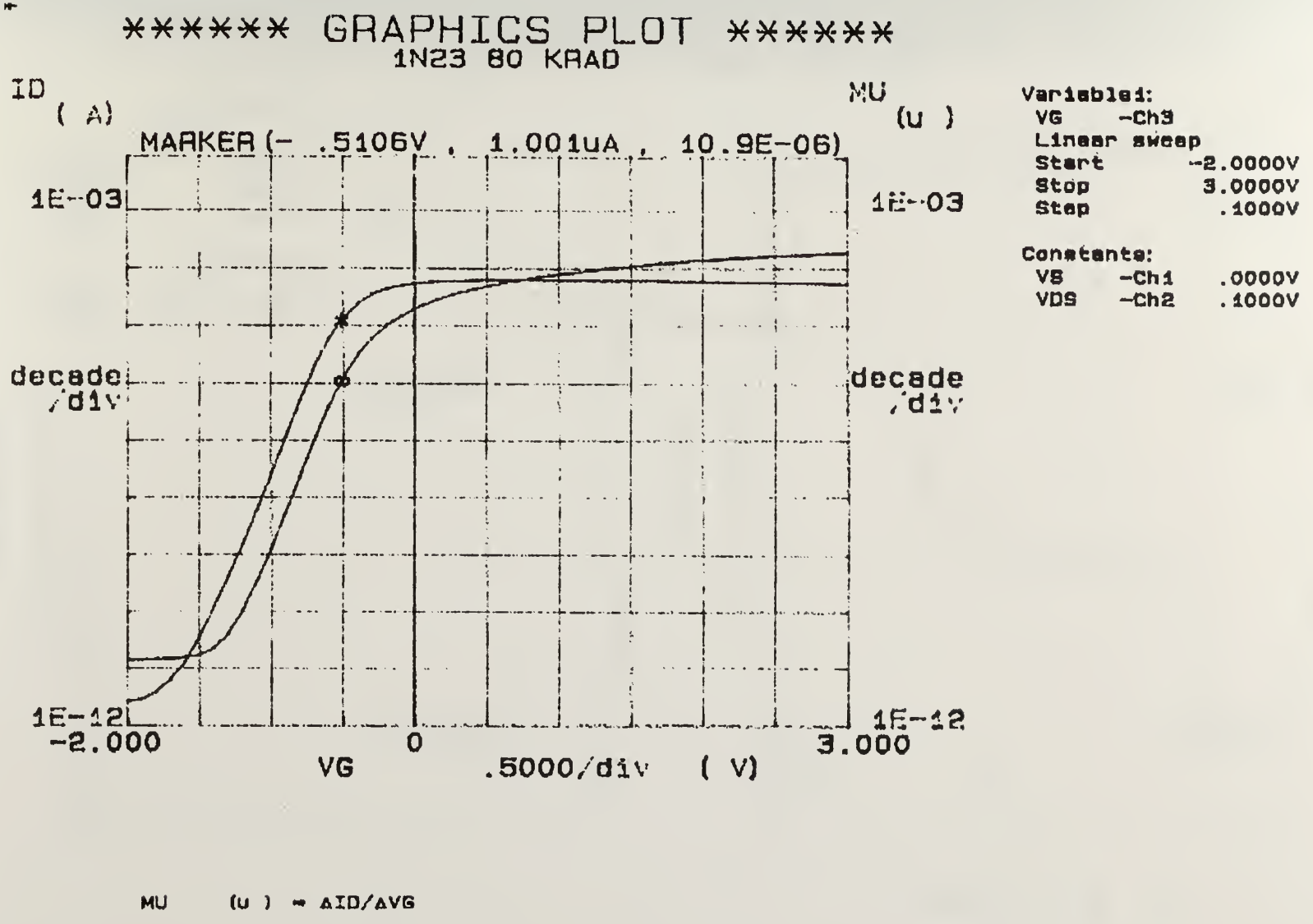
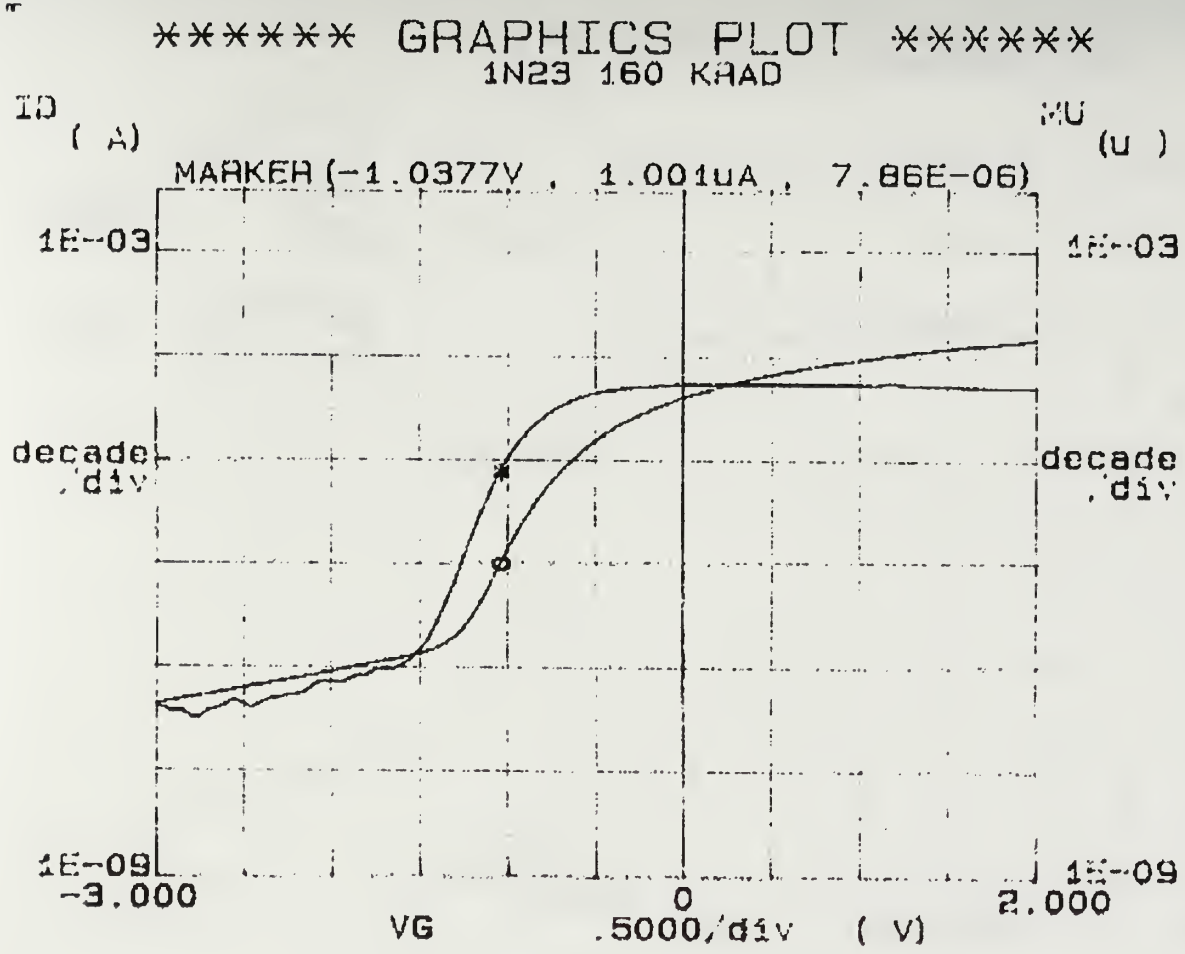

****** GRAPHICS PLOT ******
1N23 80 KRAD
ID
(A)
MU
(u)
MARKER (- .5106V , 1.001uA , 10.9E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-12
1E-12
-2.000
0
3.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -2.0000V
Stop 3.0000V
Step .1000V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = AID/AVG

Figure C.104.



Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V

Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V

Figure C.105.

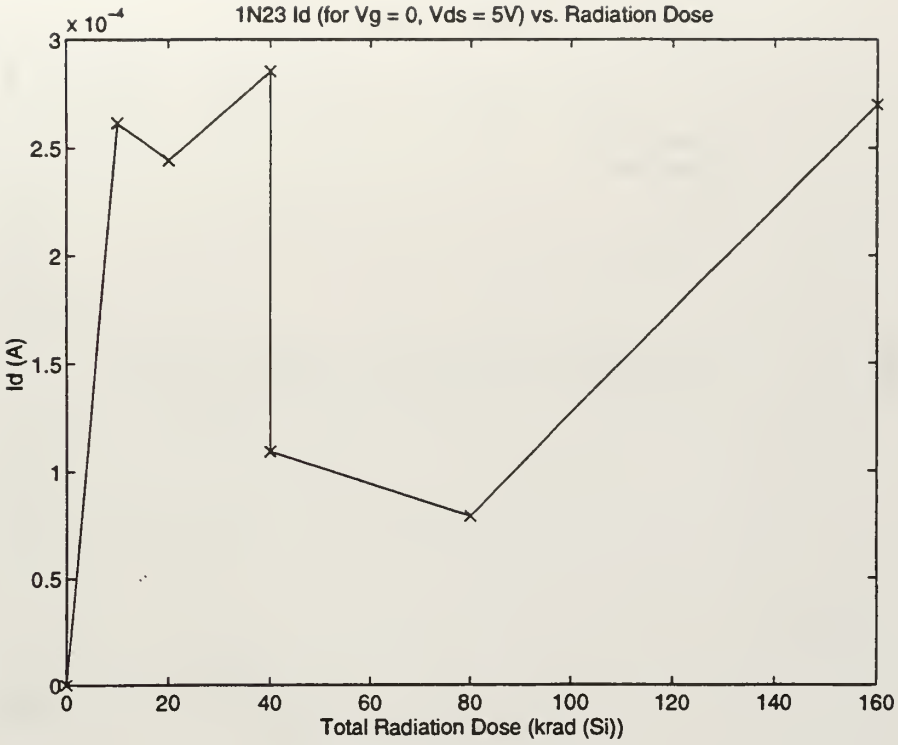


Figure C.106.

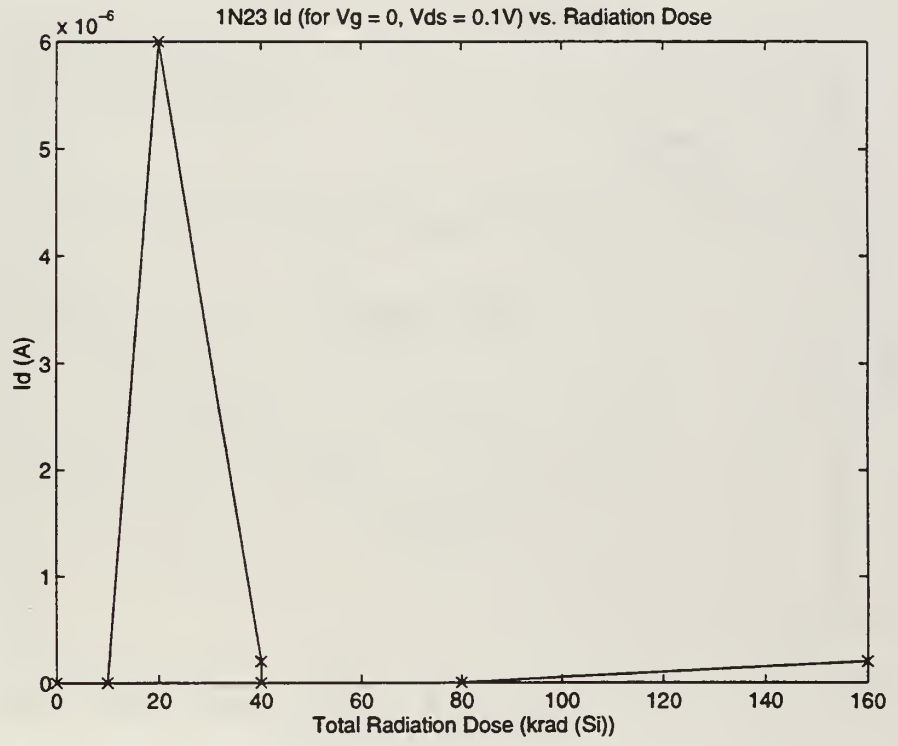


Figure C.107.

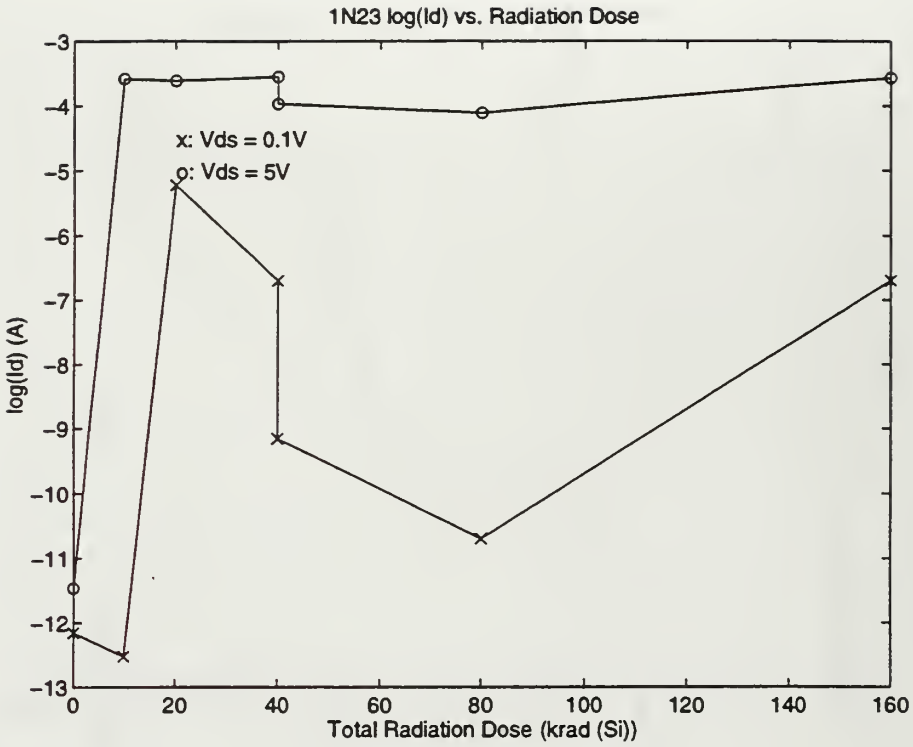


Figure C.108.

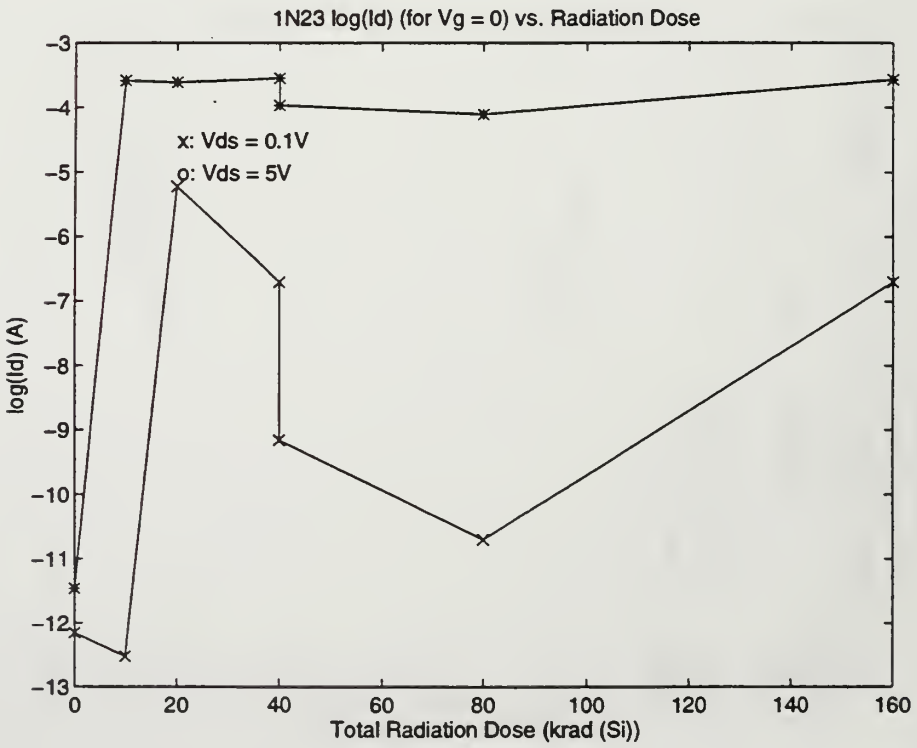


Figure C.109.

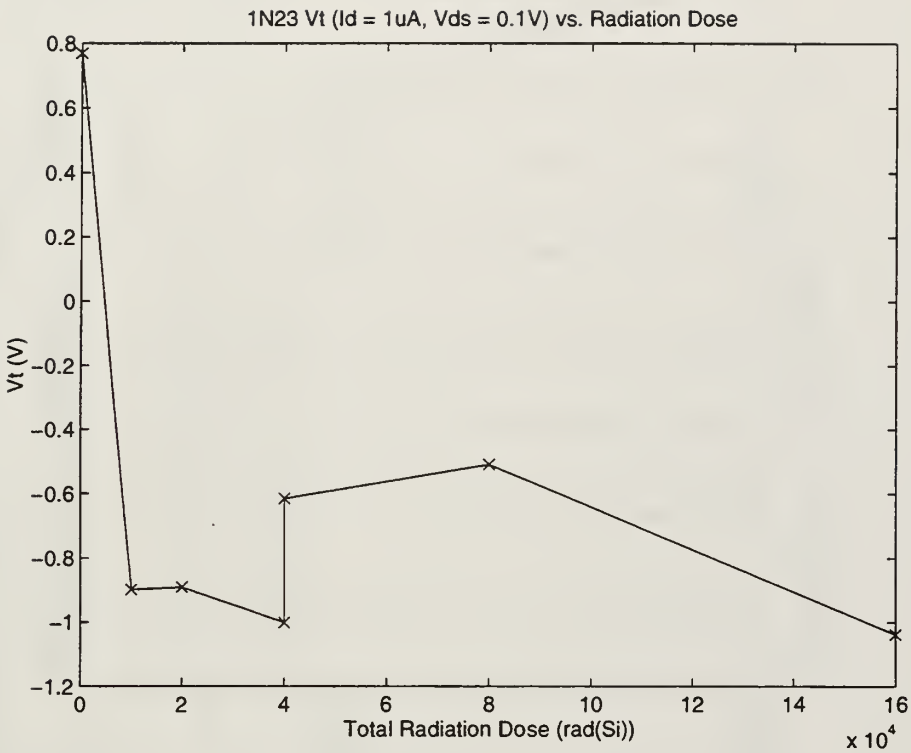

1N23 Vt (Id = 1uA, Vds = 0.1V) vs. Radiation Dose
Vt (V)
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1
−1.2
0
2
4
6
8
10
12
14
16
Total Radiation Dose (rad(Si))
x 10^4

Figure C.110.

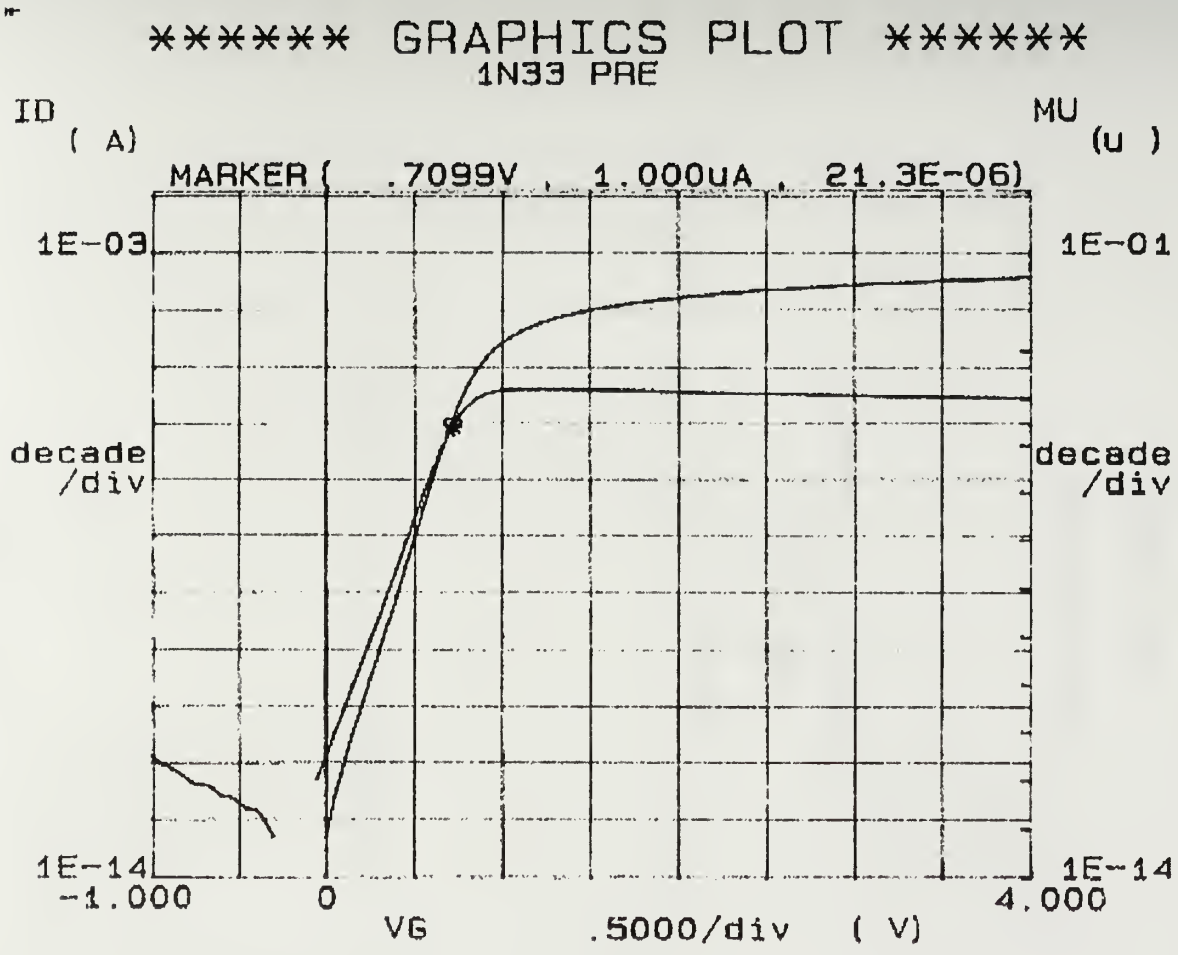

****** GRAPHICS PLOT ******
1N33 PRE
ID
(A)
MU
(u)
MARKER (.7099V , 1.000uA , 21.3E-06)
1E-03
1E-01
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.111.

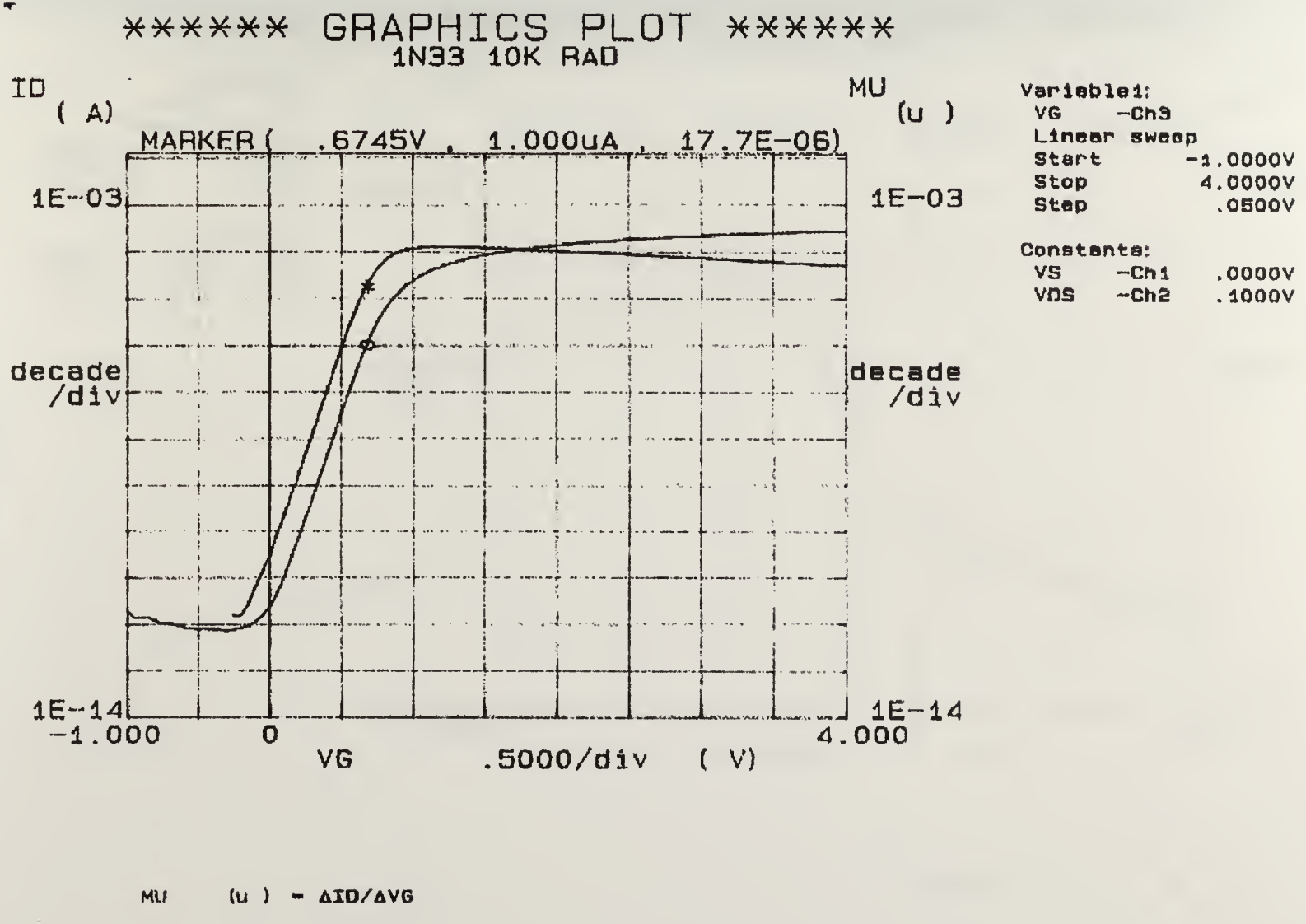

****** GRAPHICS PLOT ******
1N33 10K RAD
ID
(A)
MU
(u)
MARKER (.6745V , 1.000uA , 17.7E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-14
1E-14
-1.000
0
4.000
VG
.5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.112.

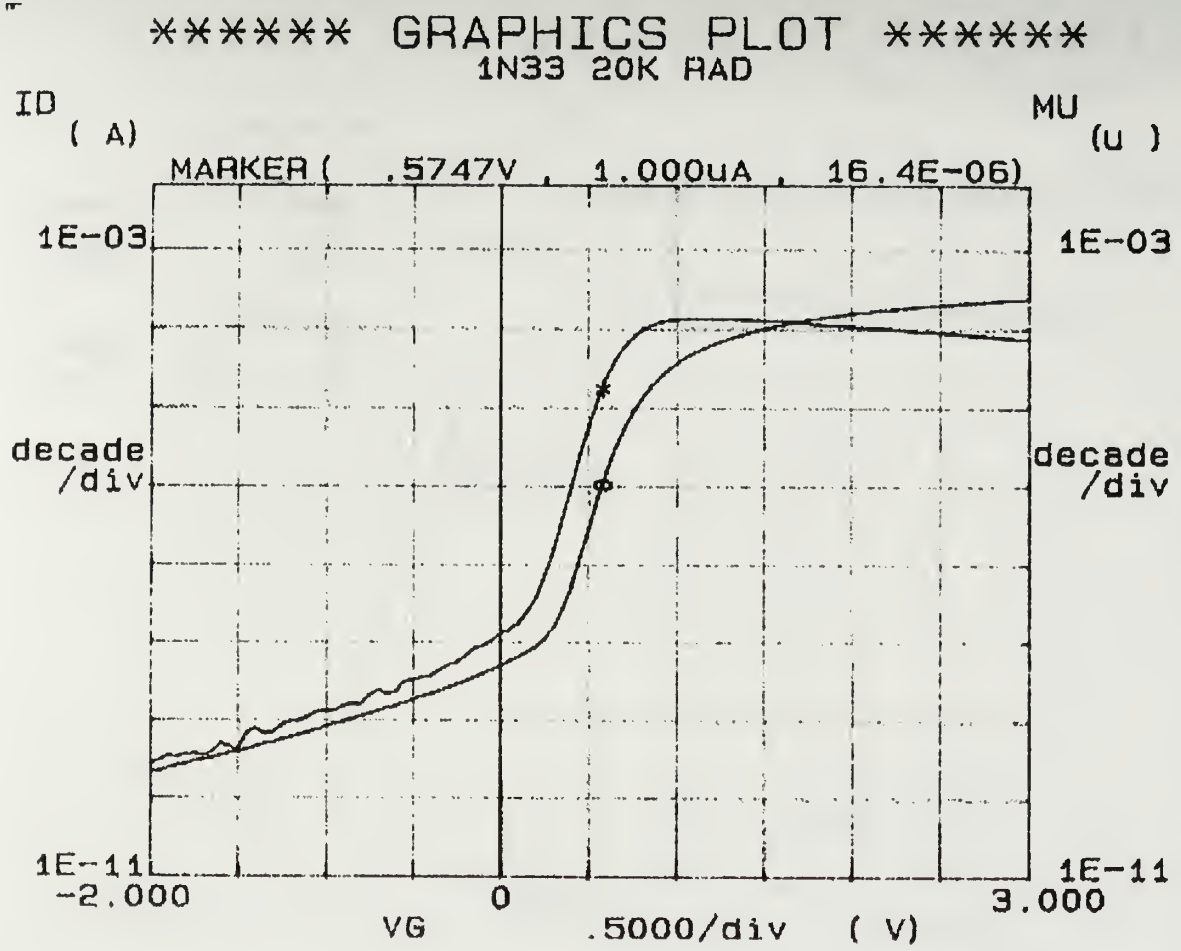

****** GRAPHICS PLOT ******
1N33 20K RAD
ID
(A)
MU
(u)
MARKER(.5747V , 1.000uA , 16.4E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-11
1E-11
-2.000
0
3.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -2.0000V
Stop 3.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.113.

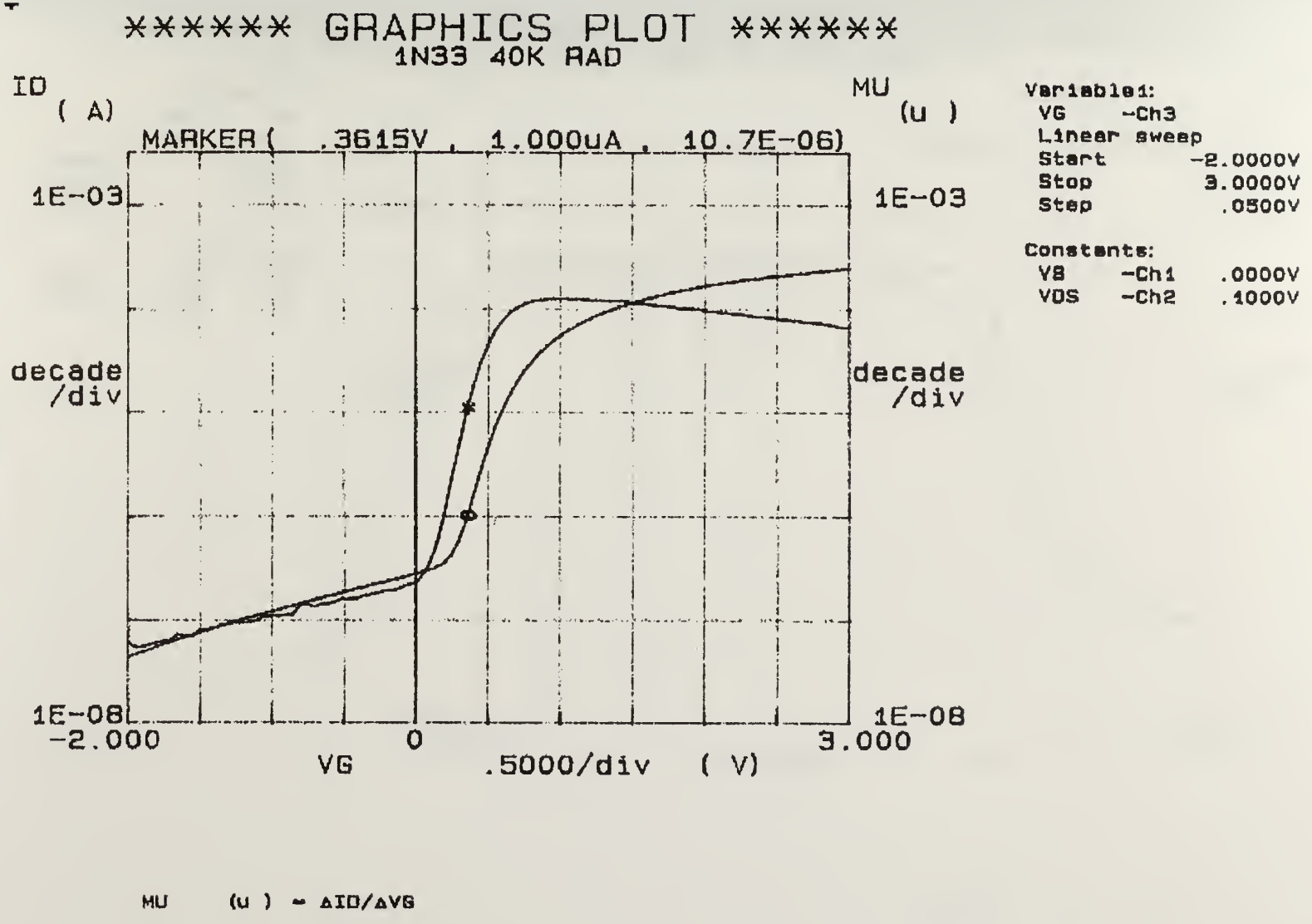

****** GRAPHICS PLOT ******
1N33 40K RAD
ID
(A)
MU
(u)
MARKER(.3615V , 1.000uA , 10.7E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-08
1E-08
-2.000
0
3.000
VG
.5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start -2.0000V
Stop 3.0000V
Step .0500V
Constants:
VB -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.114.

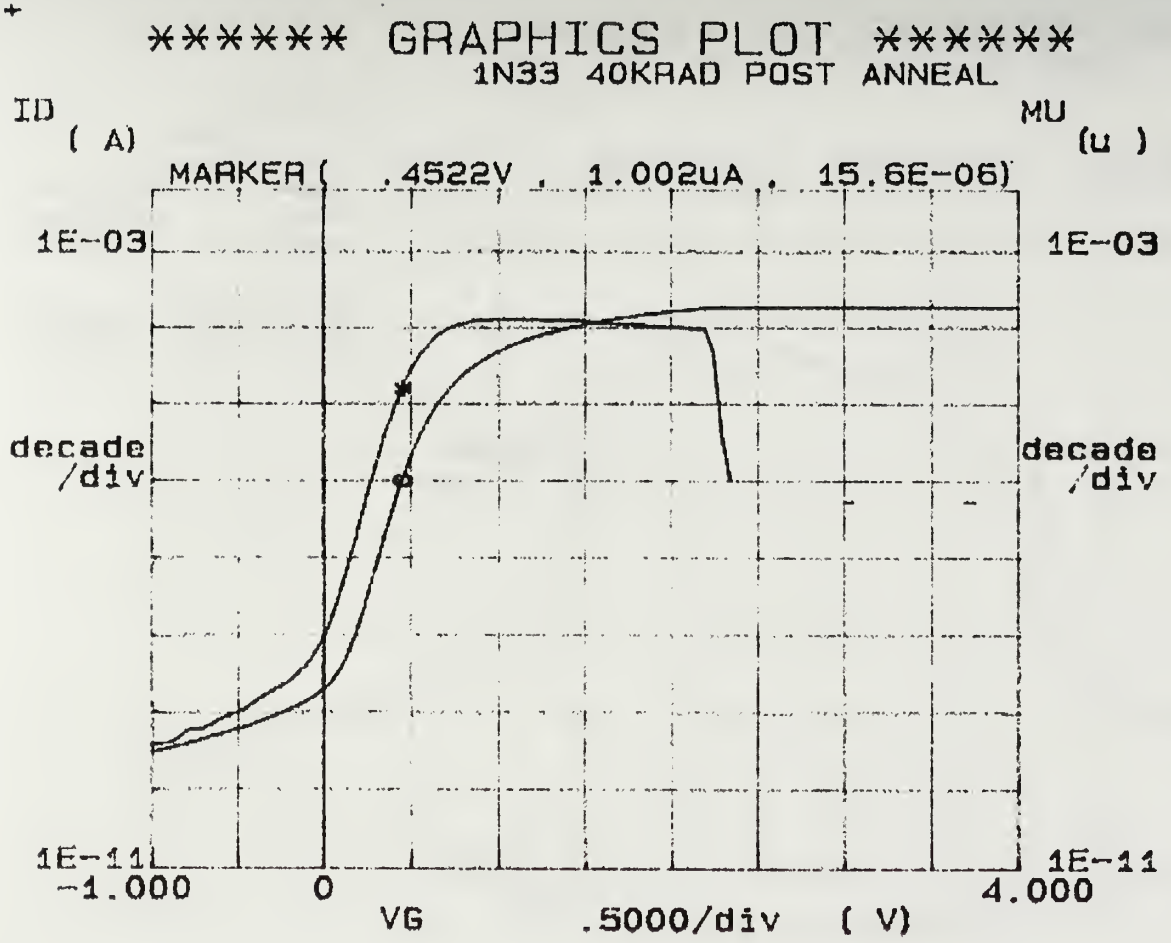

****** GRAPHICS PLOT ******
1N33 40KRAD POST ANNEAL
ID
(A)
MU
(u)
MARKER (.4522V , 1.002uA , 15.6E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-11
1E-11
-1.000
0
4.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -1.0000V
Stop 4.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = AID/AVG

Figure C.115.

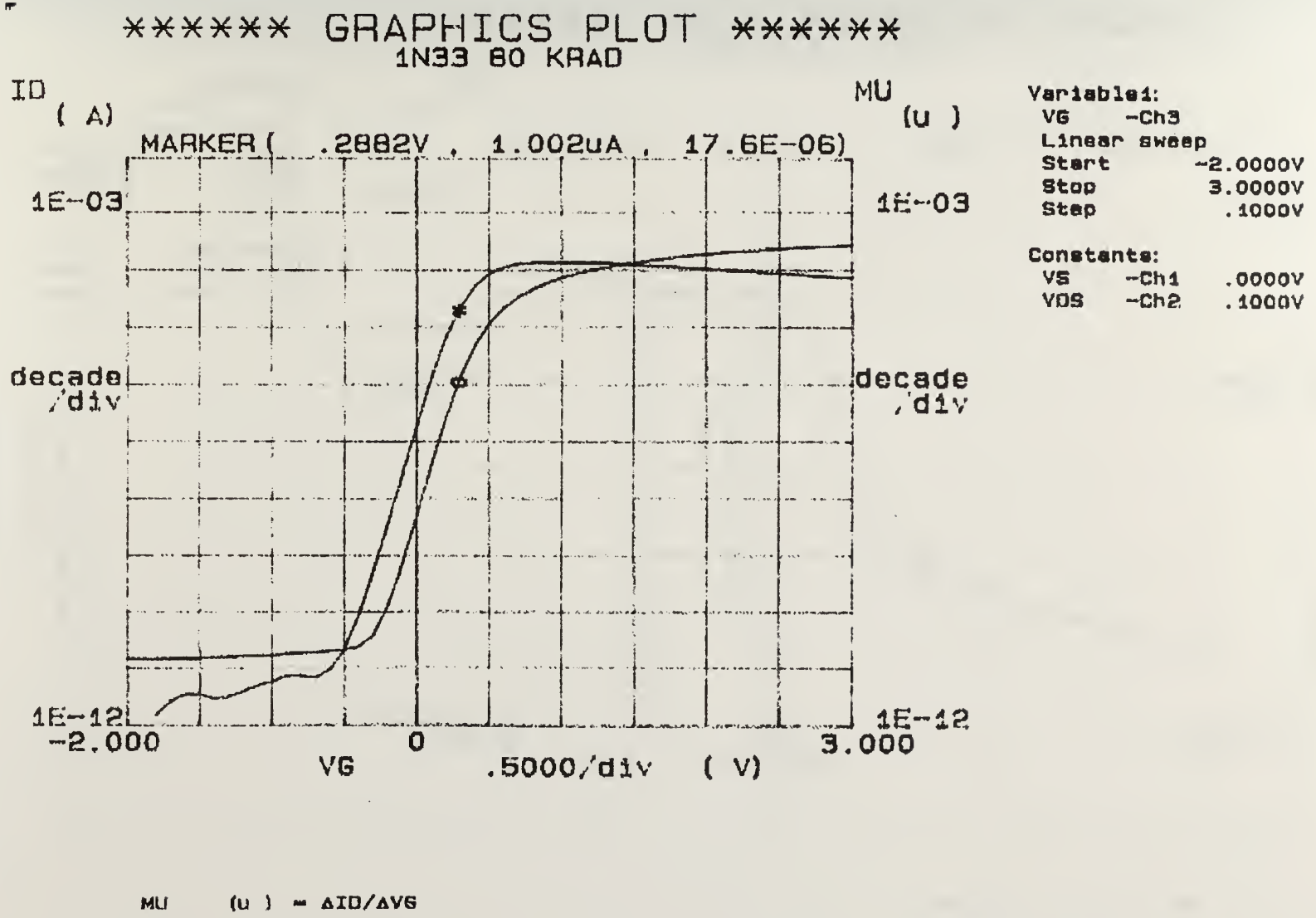

****** GRAPHICS PLOT ******
1N33 80 KRAD
ID
(A)
MU
(u)
MARKER(.2882V , 1.002uA , 17.6E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-12
1E-12
-2.000
0
3.000
VG
.5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start -2.0000V
Stop 3.0000V
Step .1000V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.116.

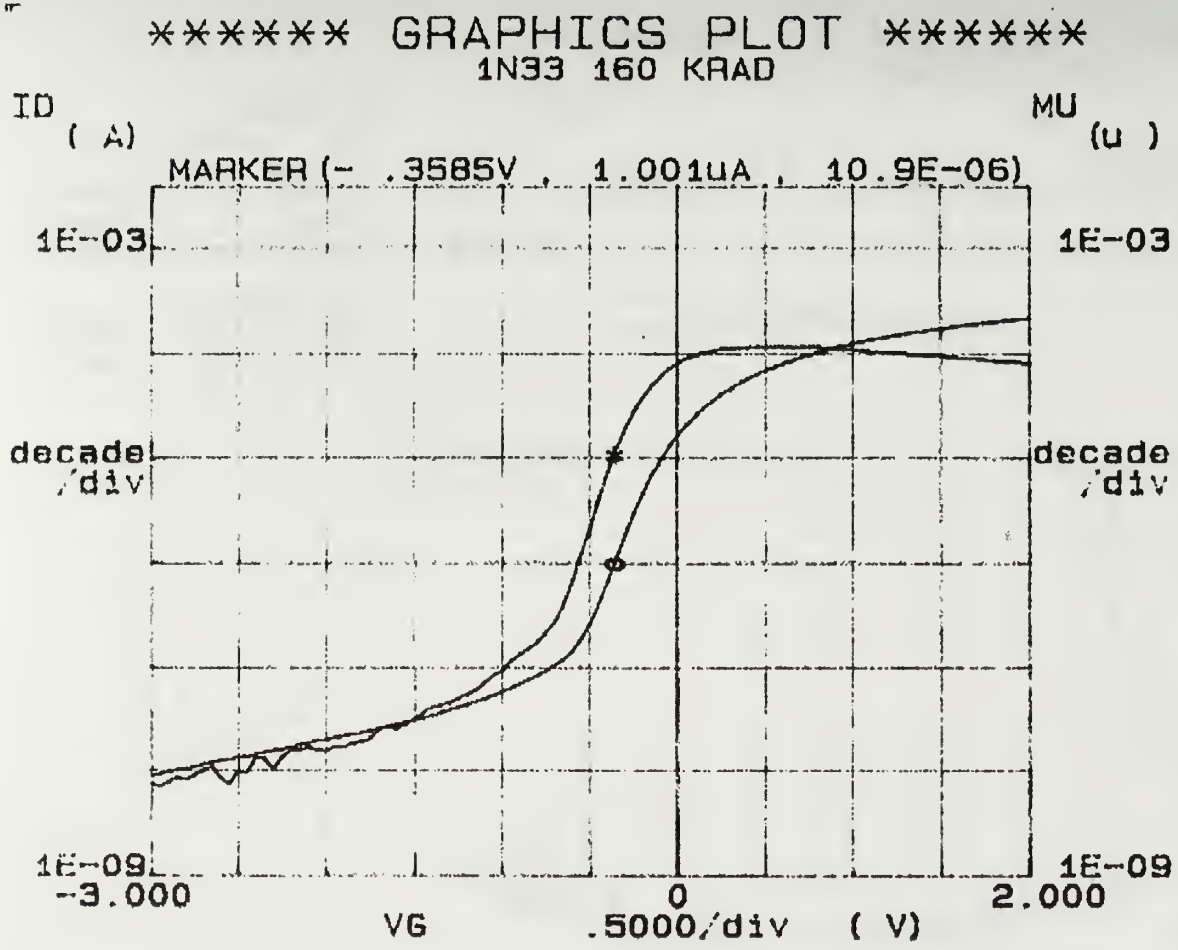

****** GRAPHICS PLOT ******
1N33 160 KRAD
ID
(A)
MU
(u)
MARKER (- .3585V , 1.001uA , 10.9E-06)
1E-03
1E-03
decade
/div
decade
/div
1E-09
1E-09
-3.000
0
2.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start -3.0000V
Stop 2.0000V
Step .0500V
Constants:
VS -Ch1 .0000V
VDS -Ch2 .1000V
MU (u) = ΔID/ΔVG

Figure C.117.

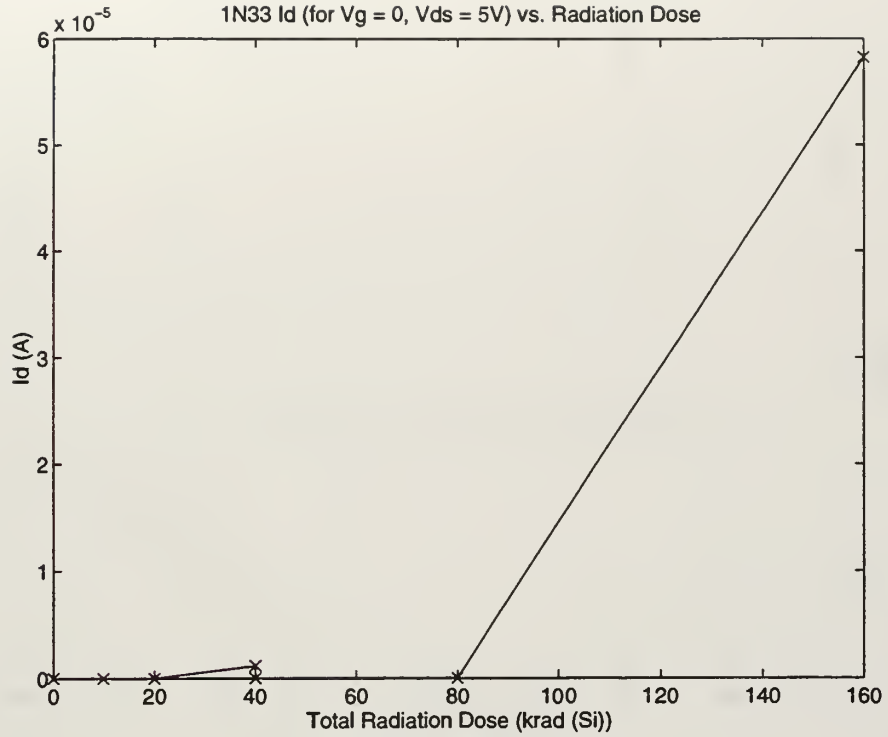


Figure C.118.

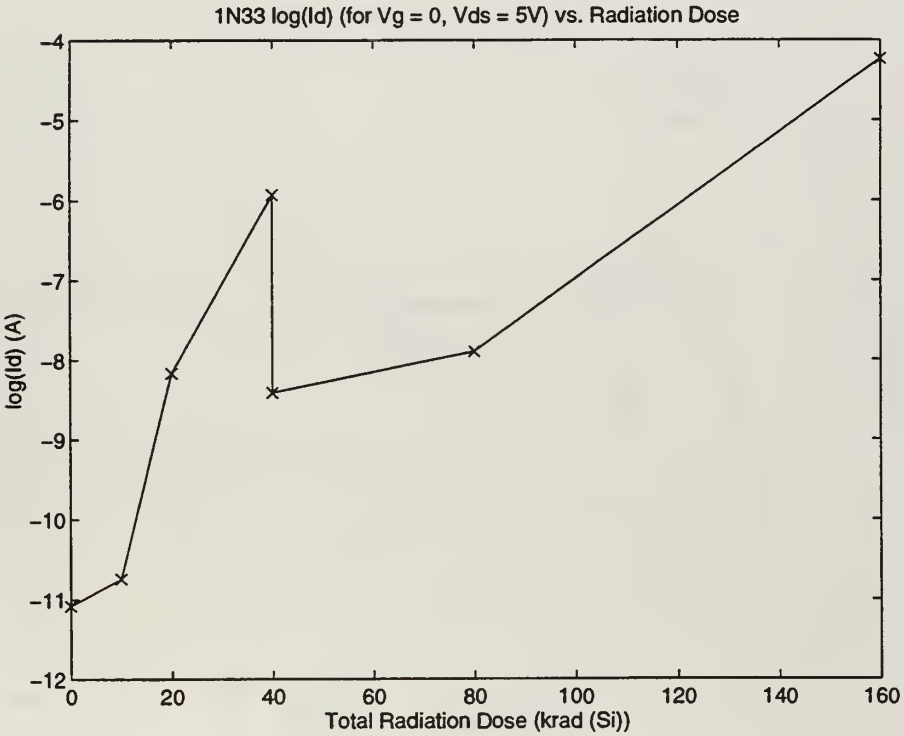


Figure C.119.

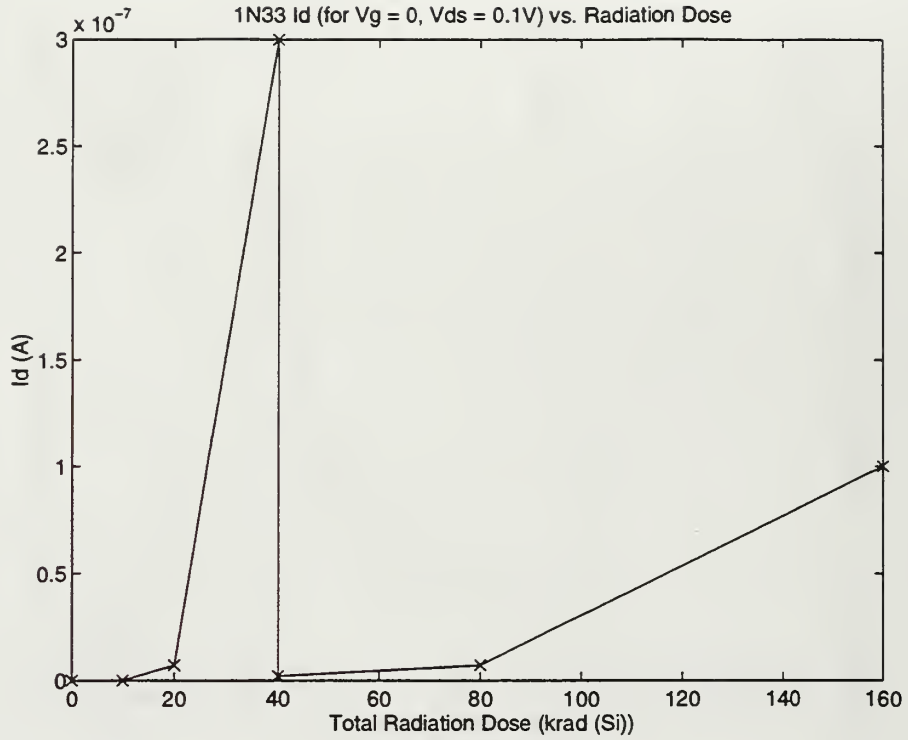


Figure C.120.

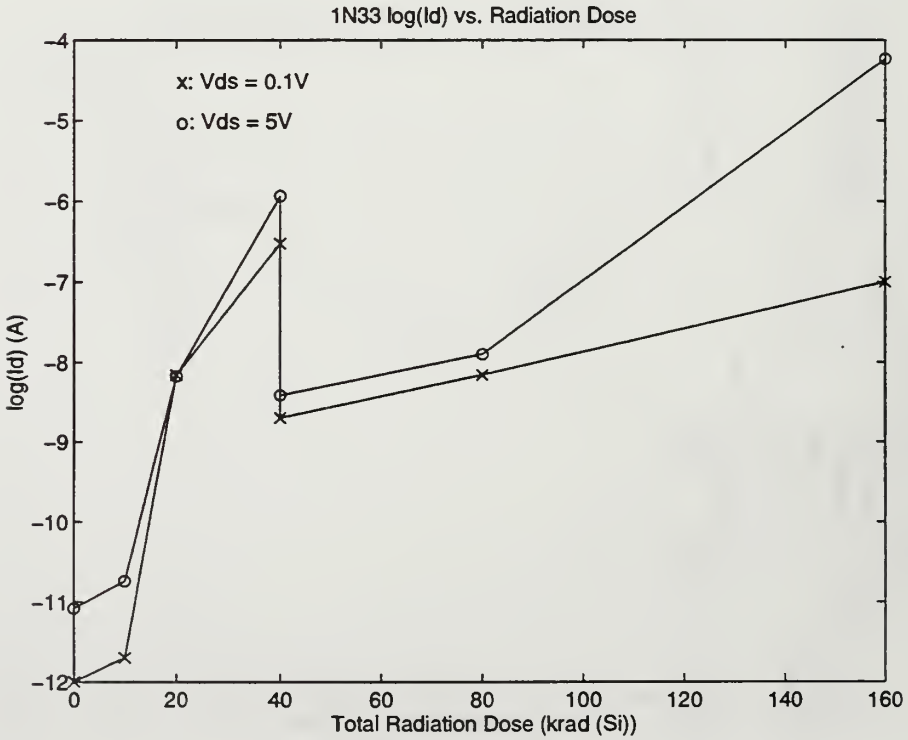


Figure C.121.

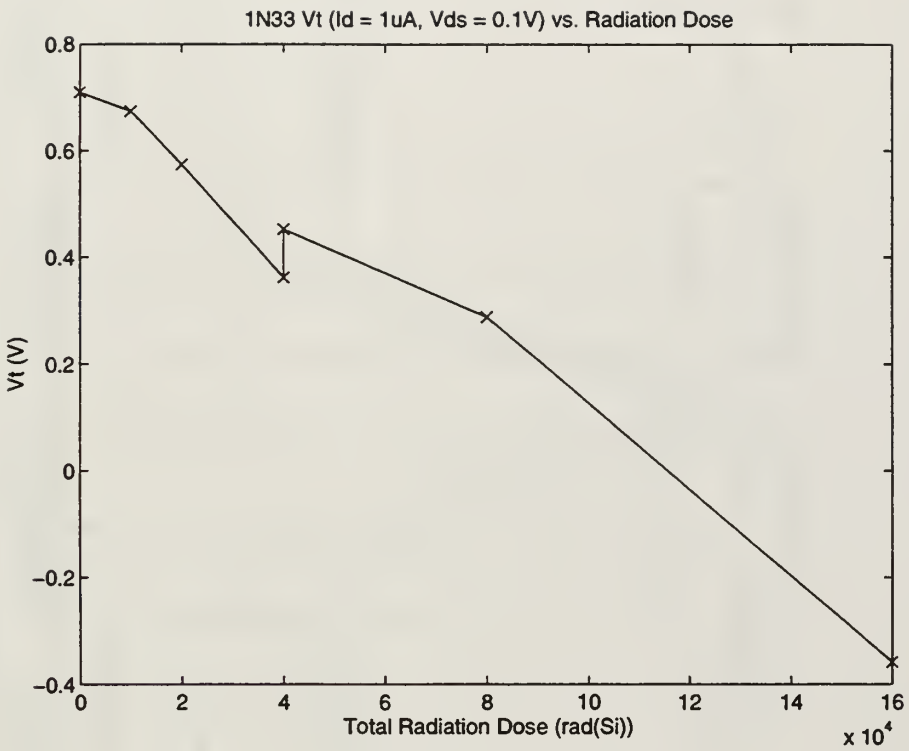
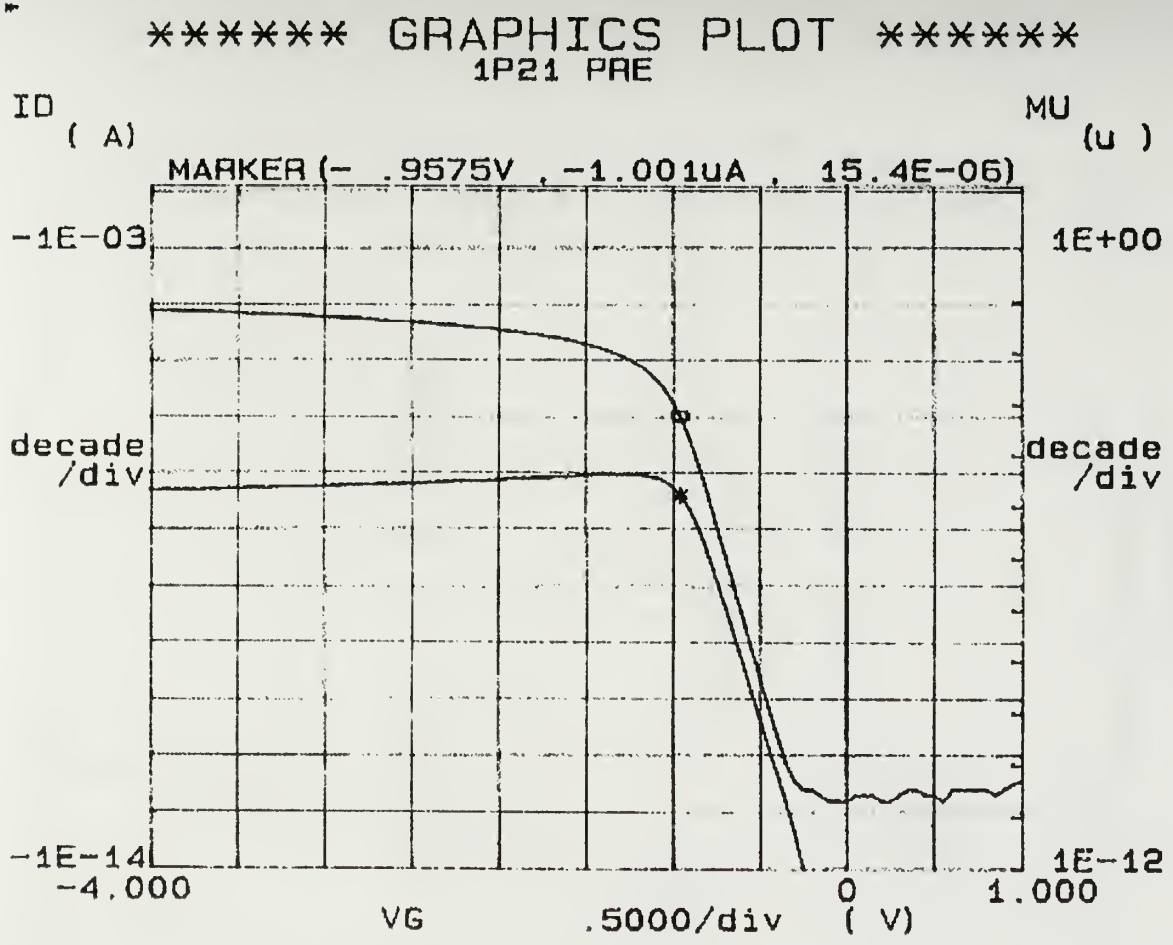

1N33 Vt (Id = 1uA, Vds = 0.1V) vs. Radiation Dose
Vt (V)
0.8
0.6
0.4
0.2
0
−0.2
−0.4
0
2
4
6
8
10
12
14
16
Total Radiation Dose (rad(Si))
x 10^4

Figure C.122.



Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V

Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V

Constants:
VS -Ch1 .0000V

Figure C.123.

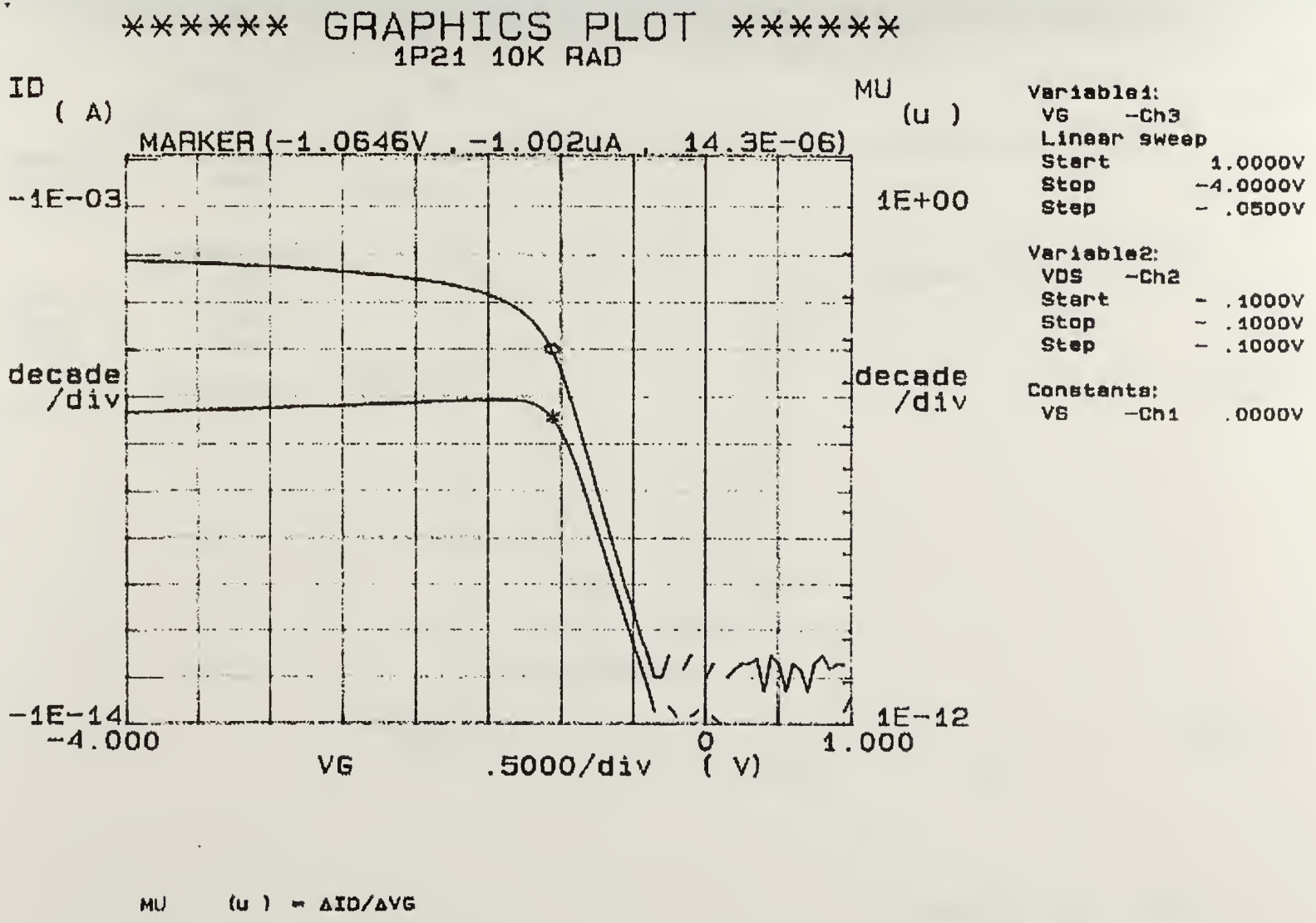

****** GRAPHICS PLOT ******
1P21 10K RAD
ID
(A)
MU
(u)
MARKER(-1.0646V , -1.002uA , 14.3E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constanta:
VG -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.124.

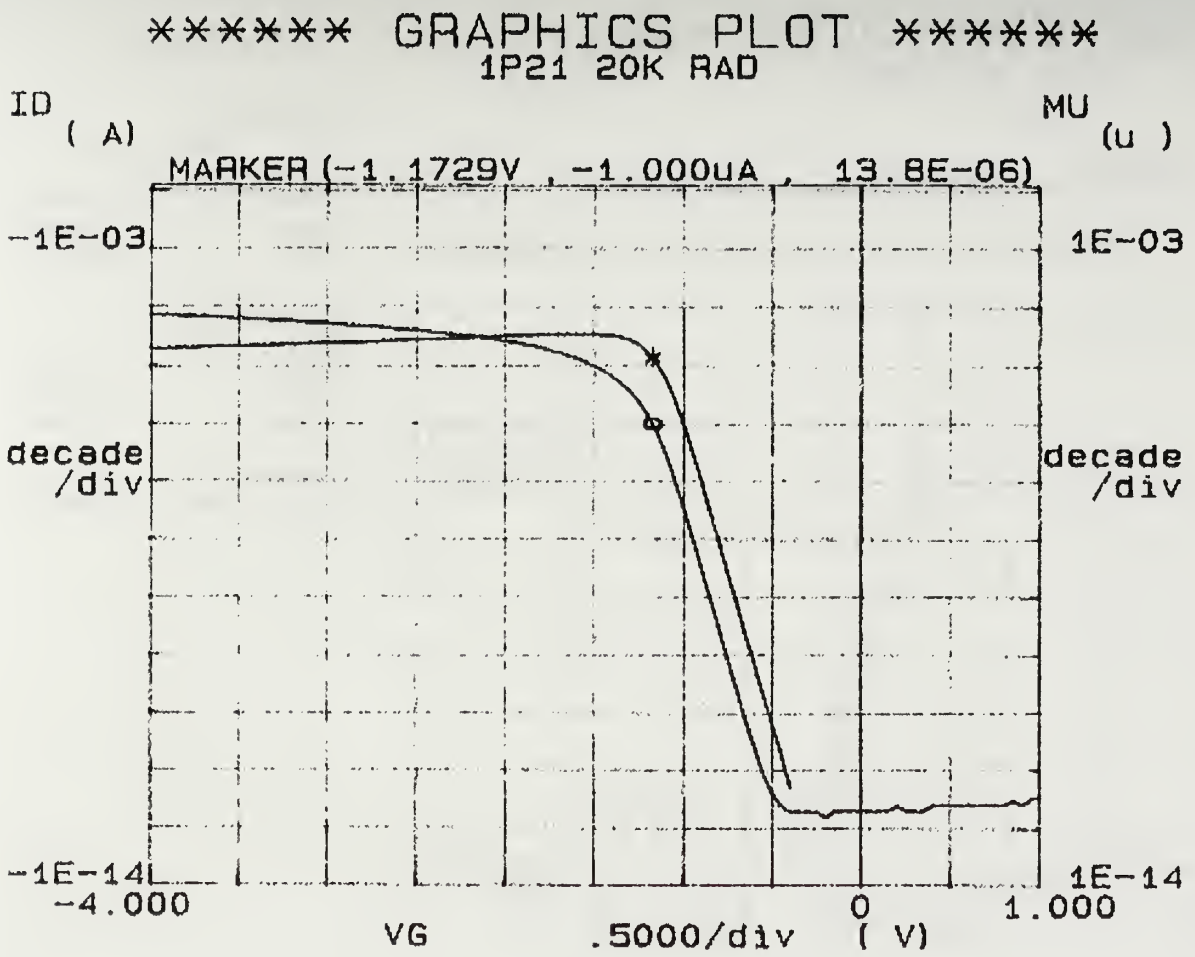

****** GRAPHICS PLOT ******
1P21 20K RAD
ID
(A)
MU
(u)
MARKER (-1.1729V , -1.000uA , 13.8E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.125.

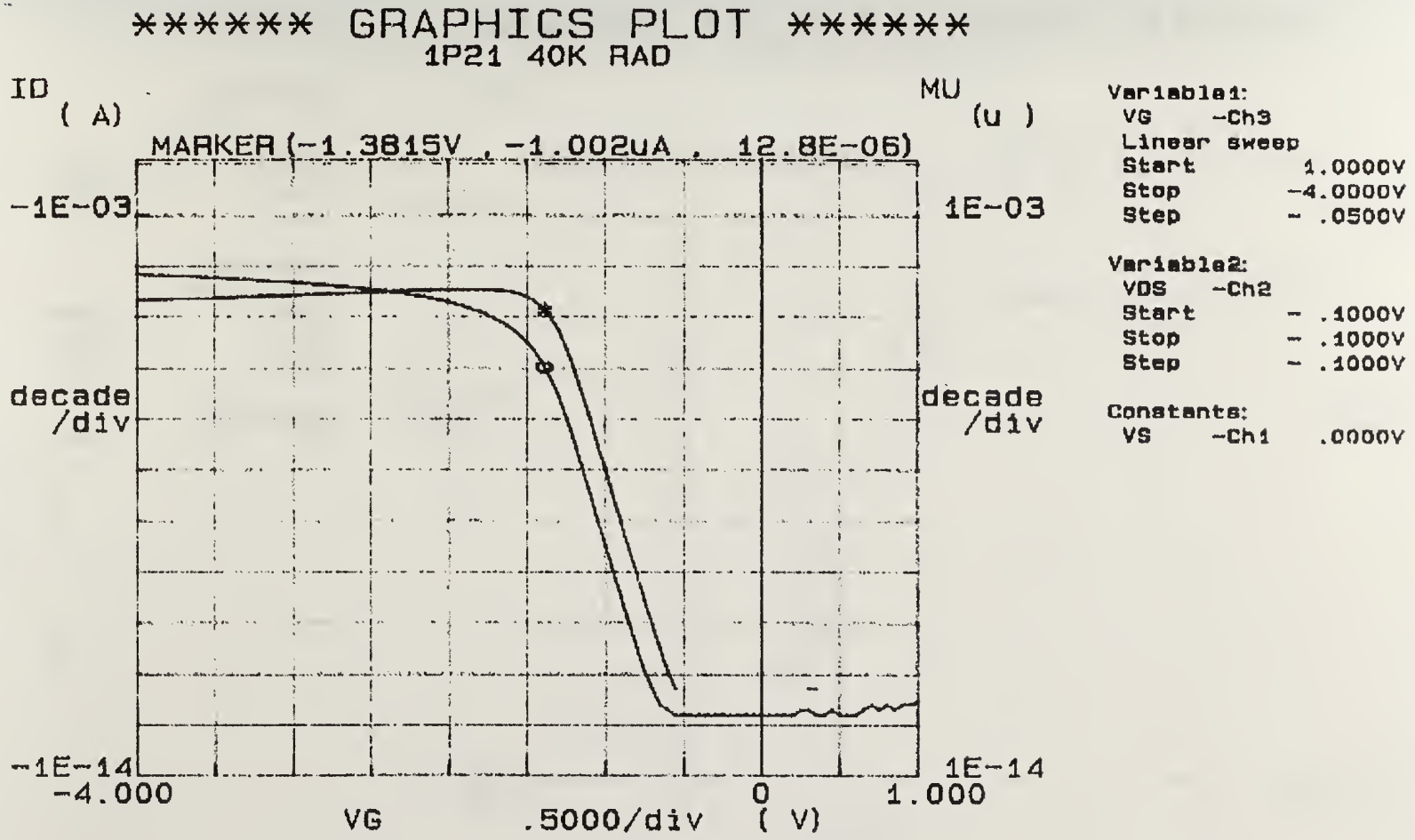

****** GRAPHICS PLOT ******
1P21 40K RAD
ID
(A)
MU
(u)
MARKER (-1.3815V , -1.002uA , 12.8E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.126.

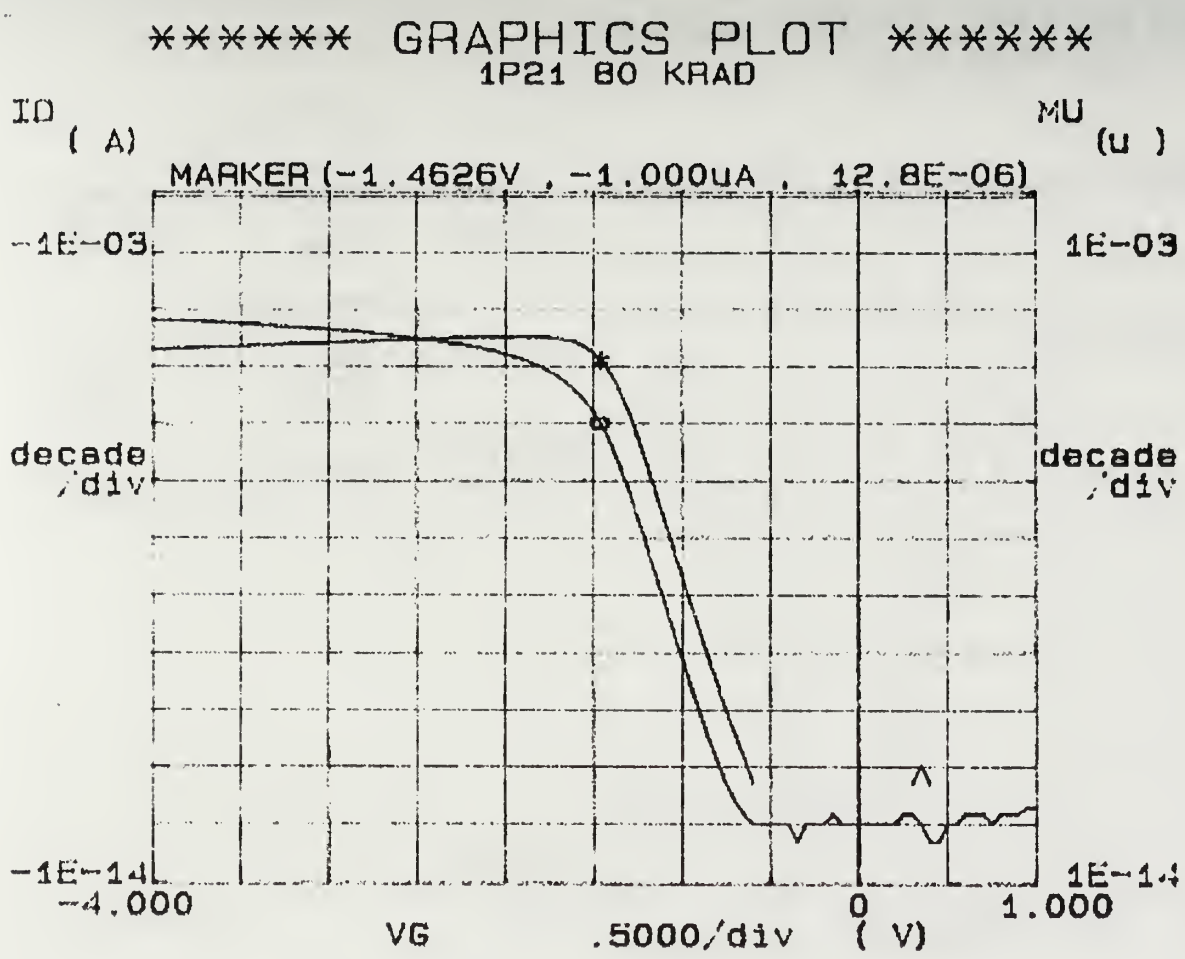

****** GRAPHICS PLOT ******
1P21 80 KRAD
ID
(A)
MU
(u)
MARKER (-1.4626V , -1.000uA , 12.8E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG .5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.127.

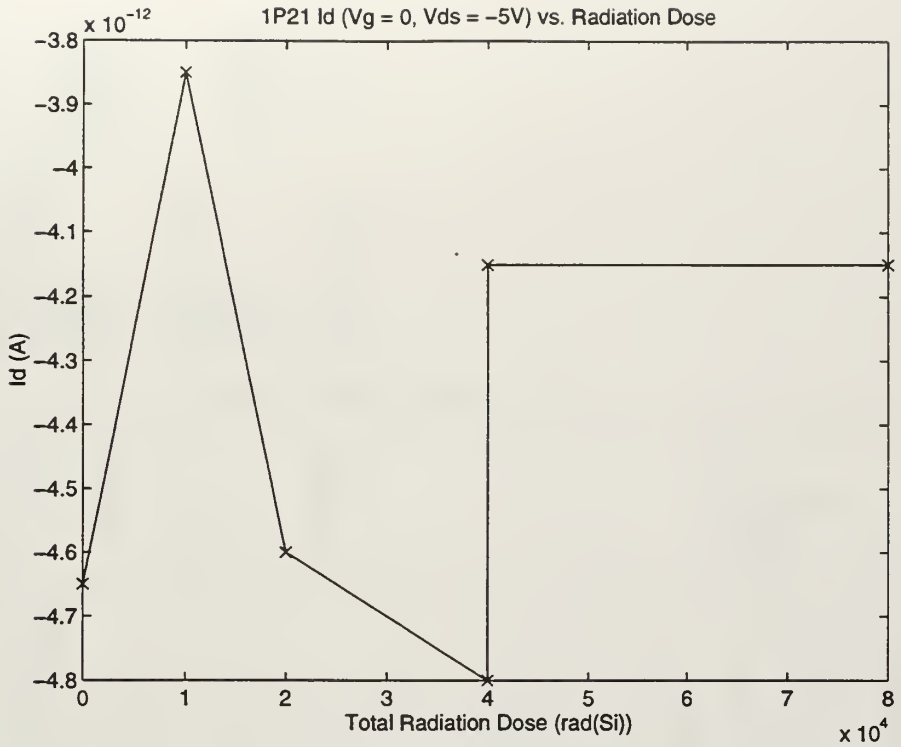


Figure C.128.

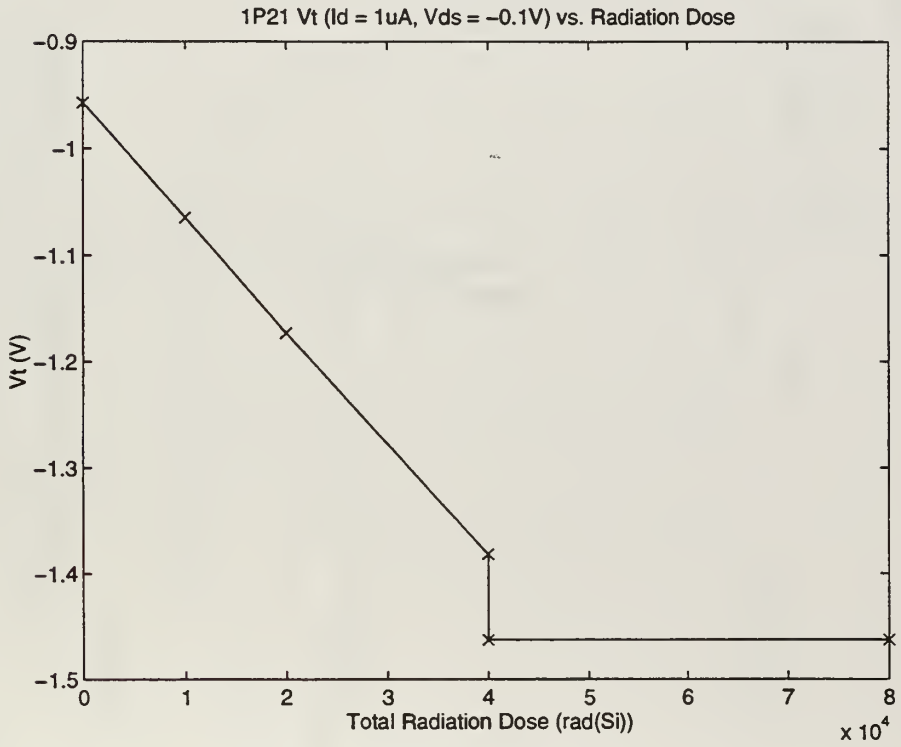
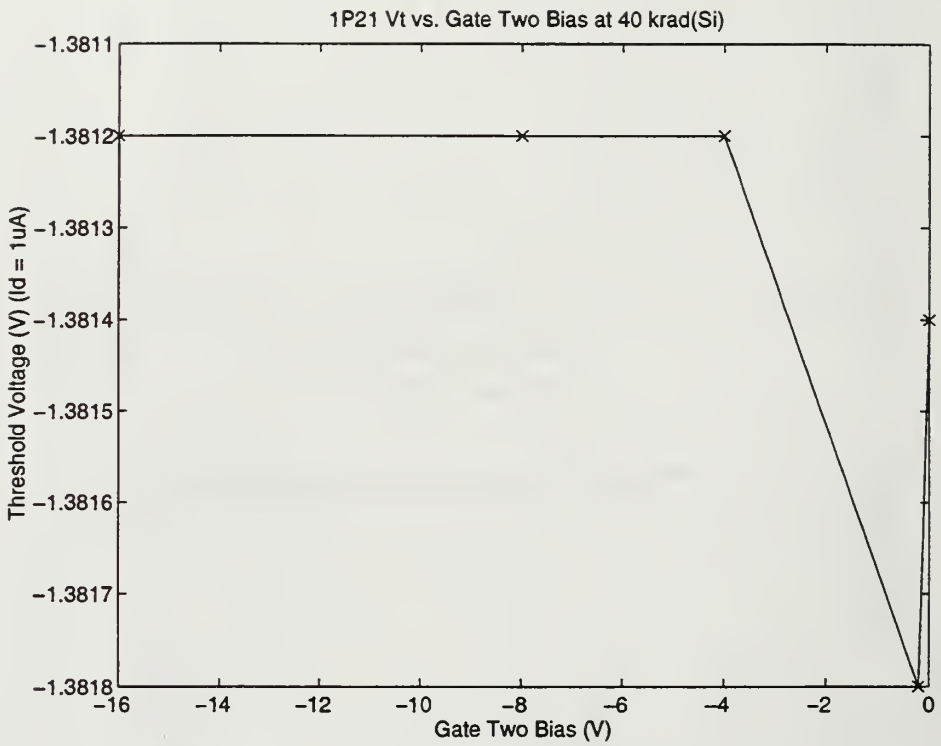


Figure C.129.


1P21 Vt vs. Gate Two Bias at 40 krad(Si)
Threshold Voltage (V) (Id = 1uA)
-1.3811
-1.3812
-1.3813
-1.3814
-1.3815
-1.3816
-1.3817
-1.3818
-16
-14
-12
-10
-8
-6
-4
-2
0
Gate Two Bias (V)
Figure C.130.

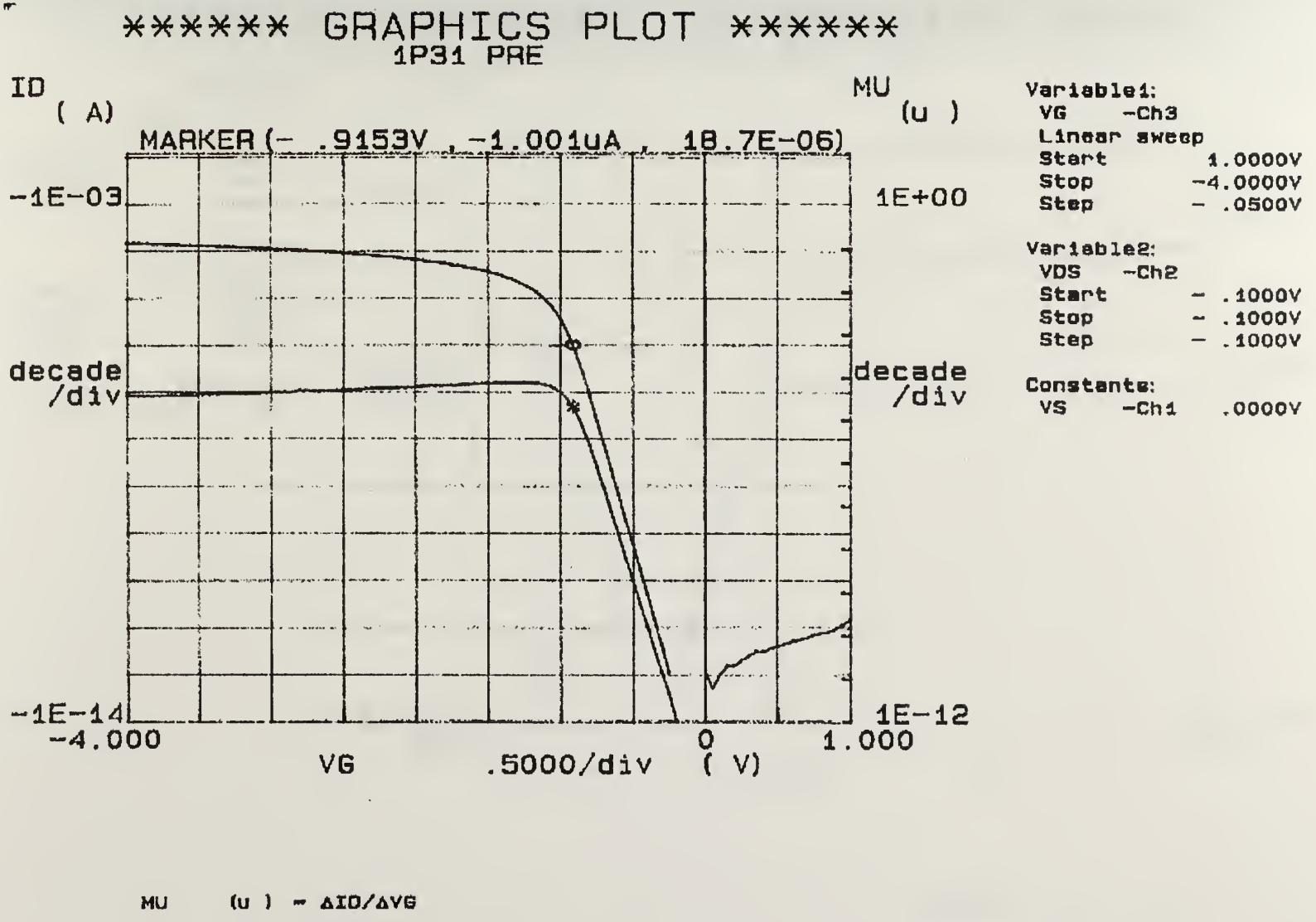

****** GRAPHICS PLOT ******
1P31 PRE
ID
(A)
MU
(u)
MARKER (- .9153V , -1.001uA , 18.7E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.131.

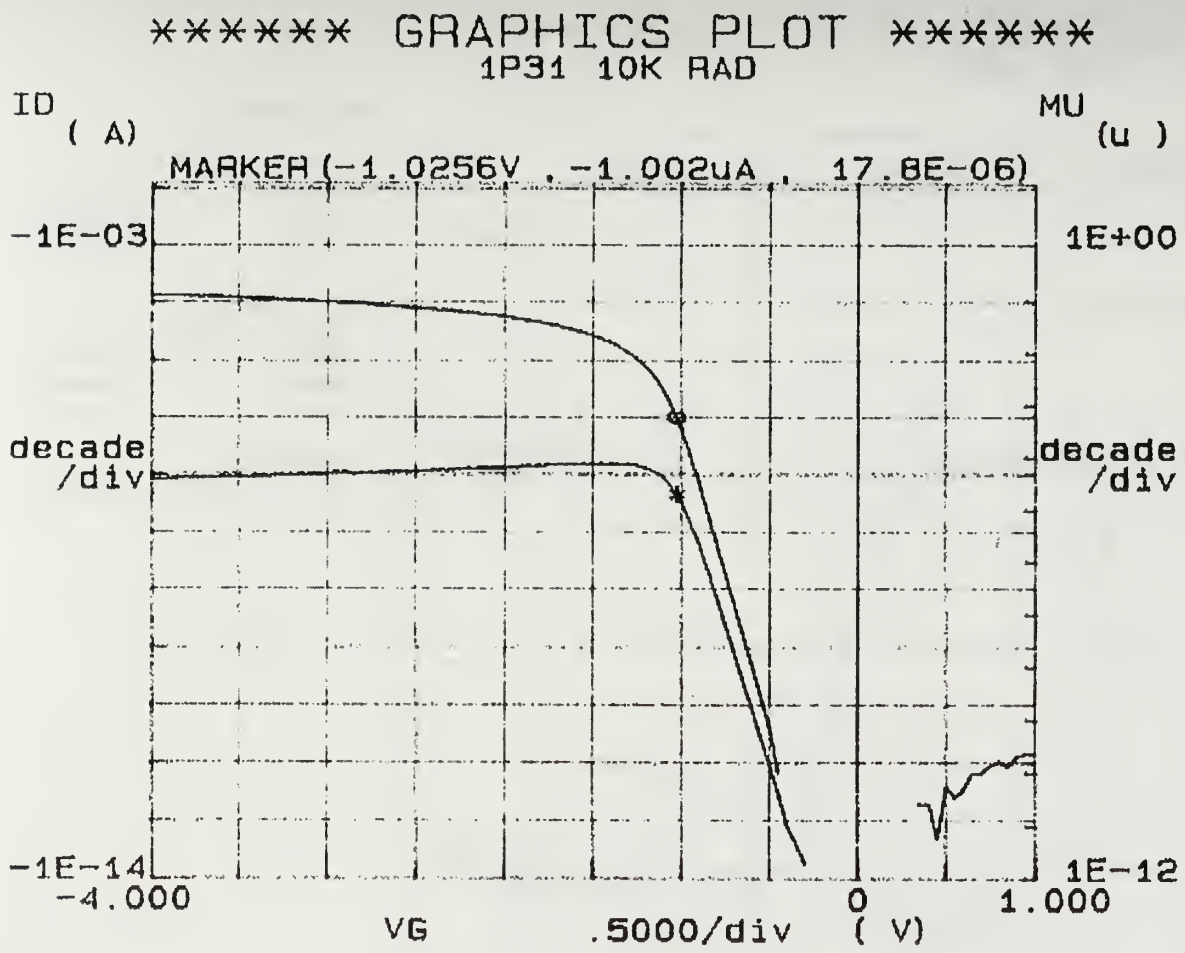

****** GRAPHICS PLOT ******
1P31 10K RAD
ID
(A)
MU
(u)
MARKER (-1.0256V , -1.002uA , 17.8E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.132.

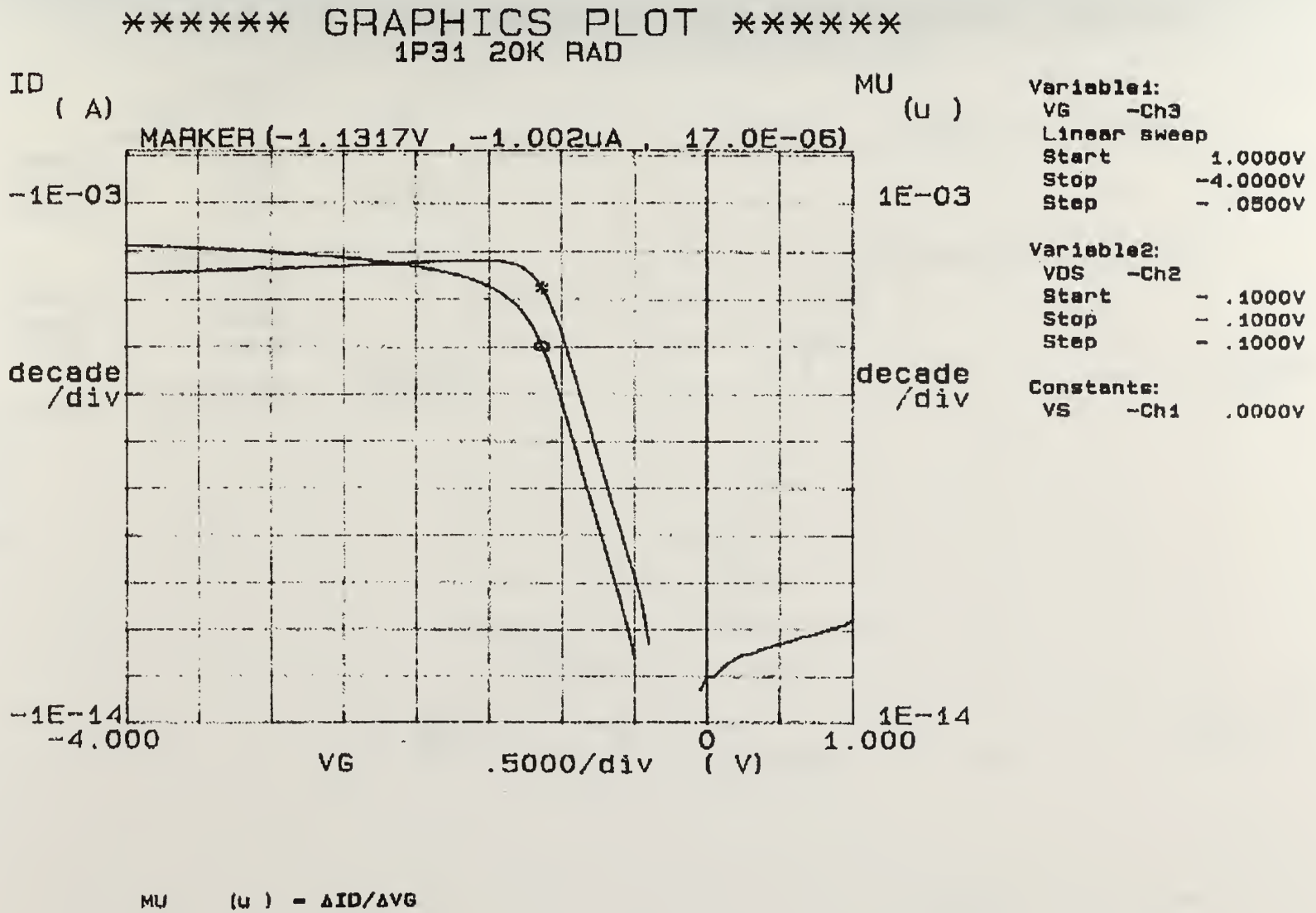
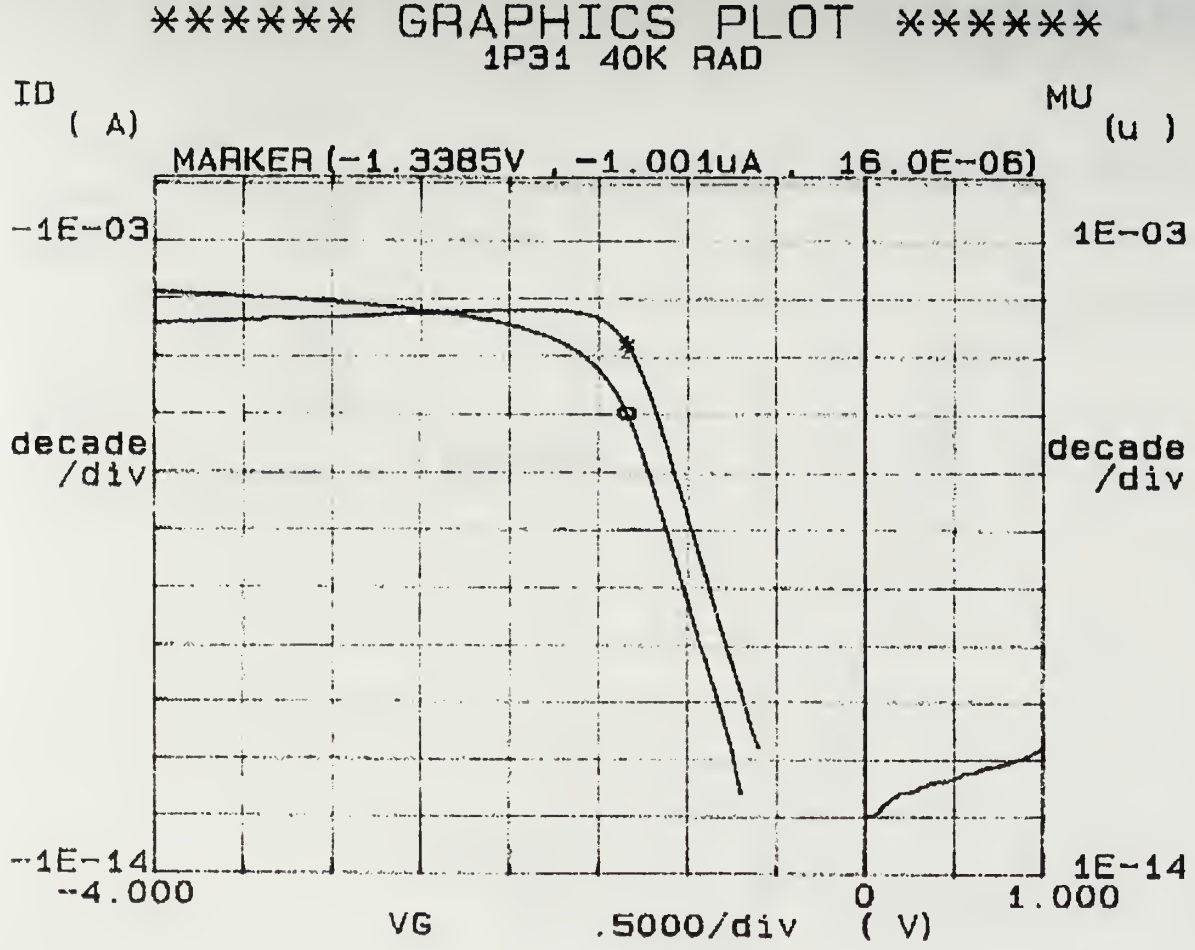

****** GRAPHICS PLOT ******
1P31 20K RAD
ID
(A)
MU
(u)
MARKER (-1.1317V , -1.002uA , 17.0E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.133.



Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V

Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V

Constants:
VS -Ch1 .0000V

Figure C.134.

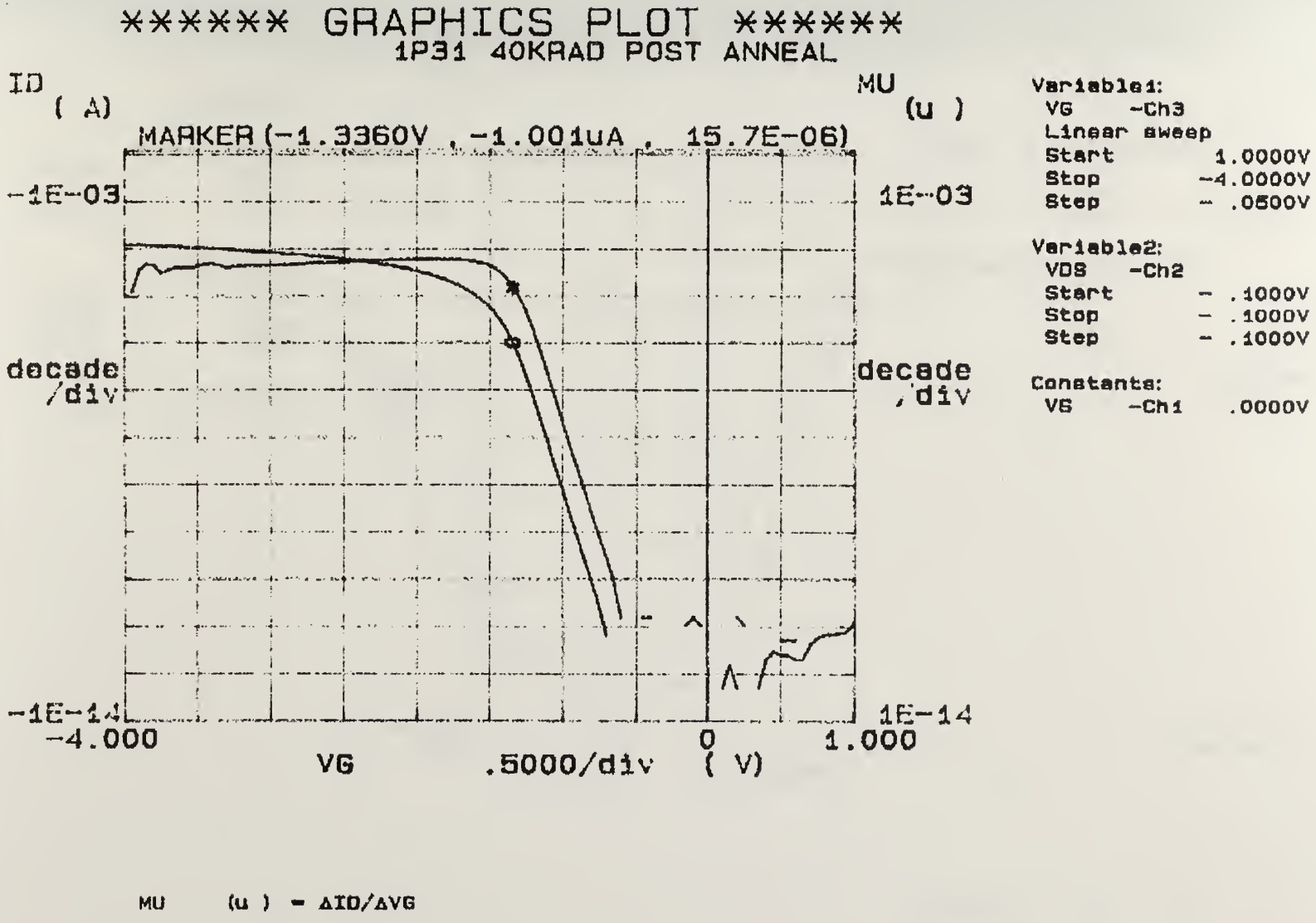

****** GRAPHICS PLOT ******
1P31 40KRAD POST ANNEAL
ID
(A)
MU
(u)
MARKER (-1.3360V , -1.001uA , 15.7E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.135.

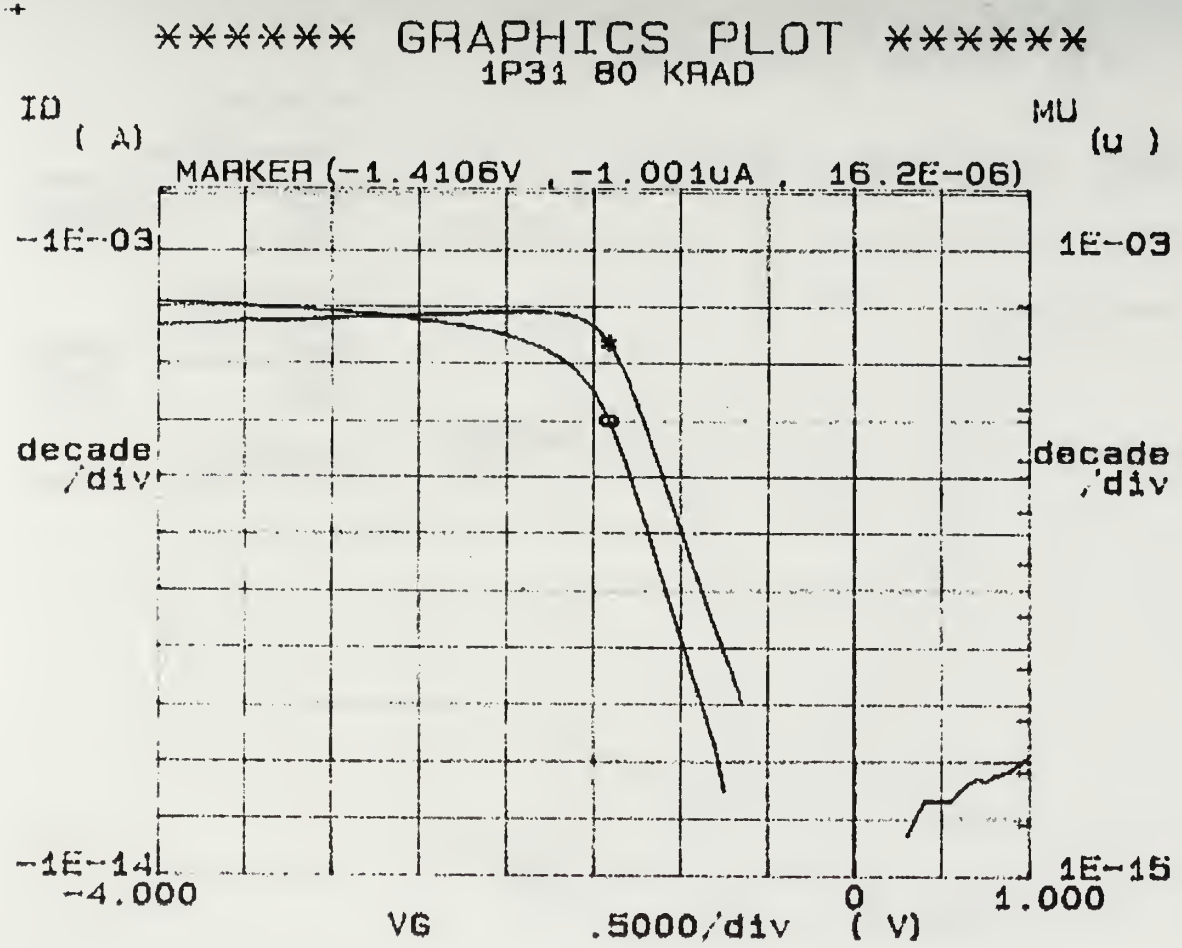

****** GRAPHICS PLOT ******
1P31 80 KRAD
ID
(A)
MU
(u)
MARKER (-1.4106V , -1.001uA , 16.2E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-15
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.136.

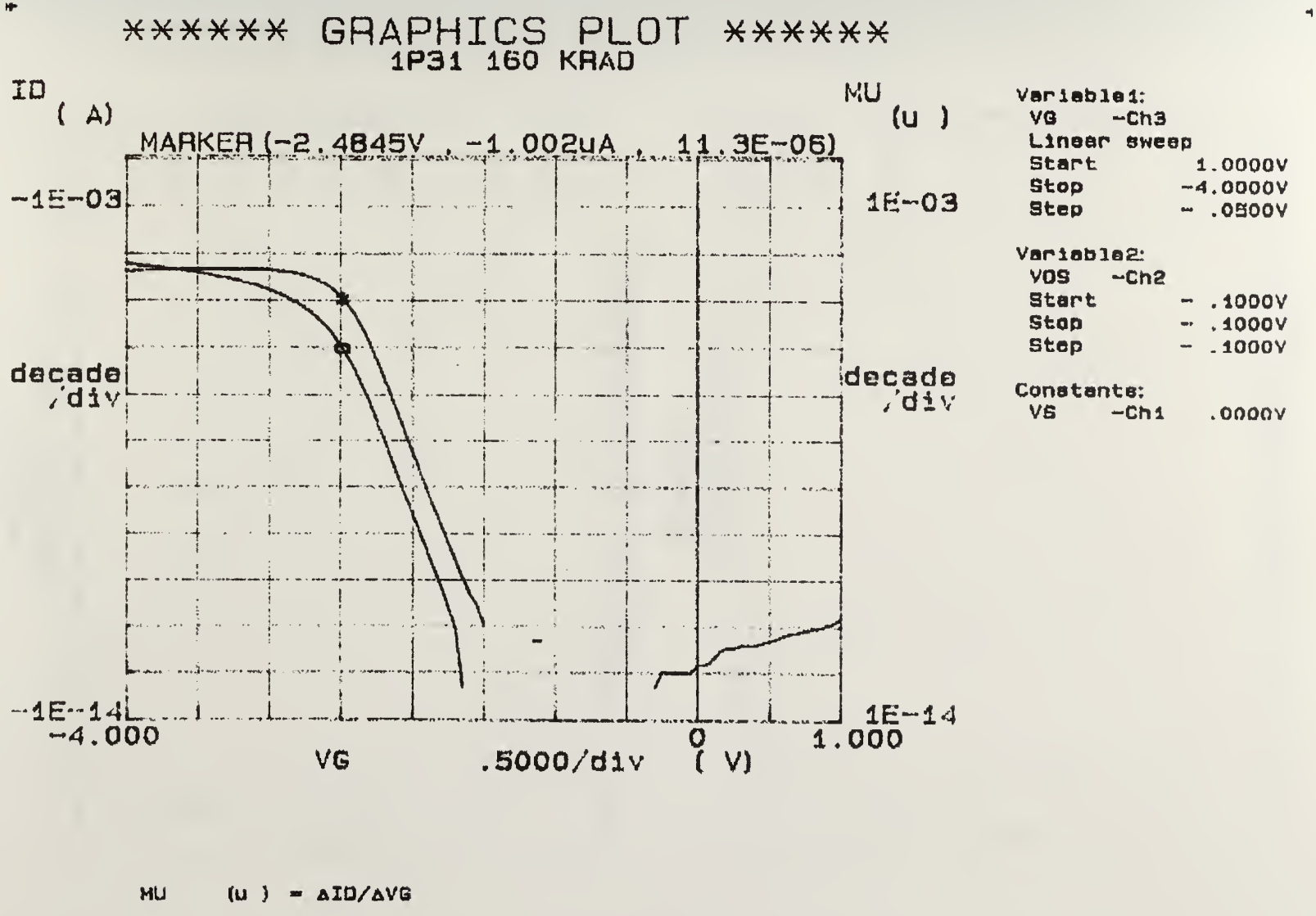

****** GRAPHICS PLOT ******
1P31 160 KRAD
ID
(A)
MU
(u)
MARKER(-2.4845V , -1.002uA , 11.3E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.137.

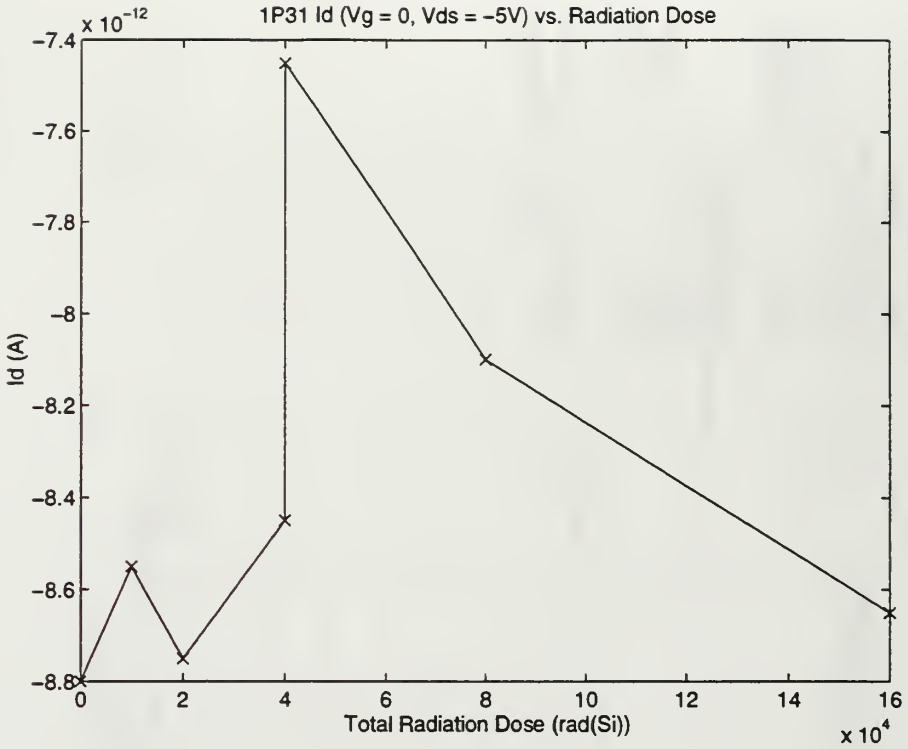


Figure C.138.

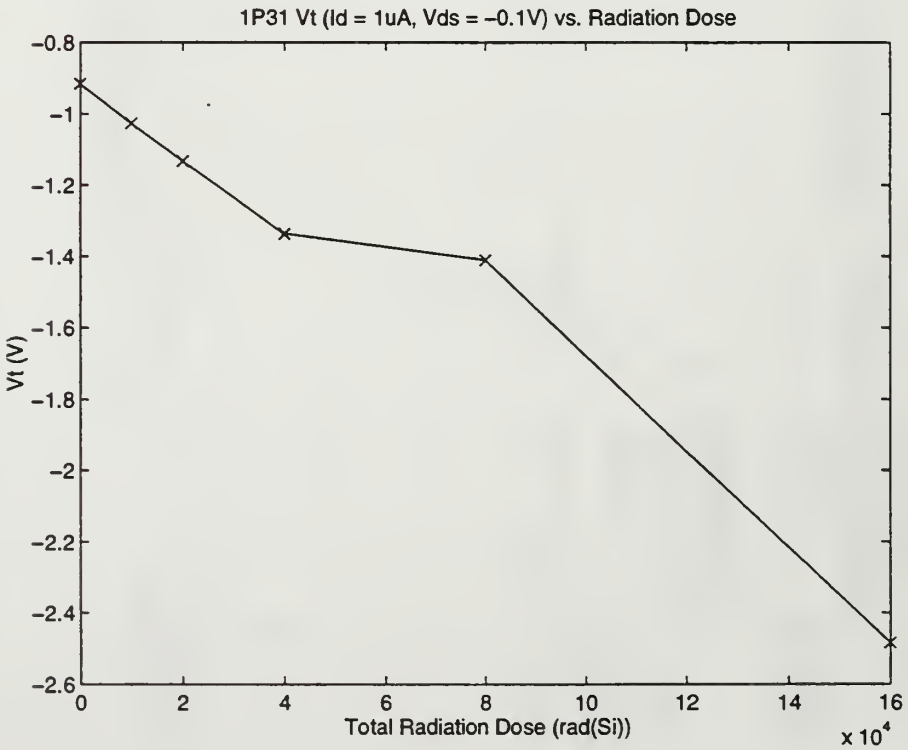


Figure C.139.

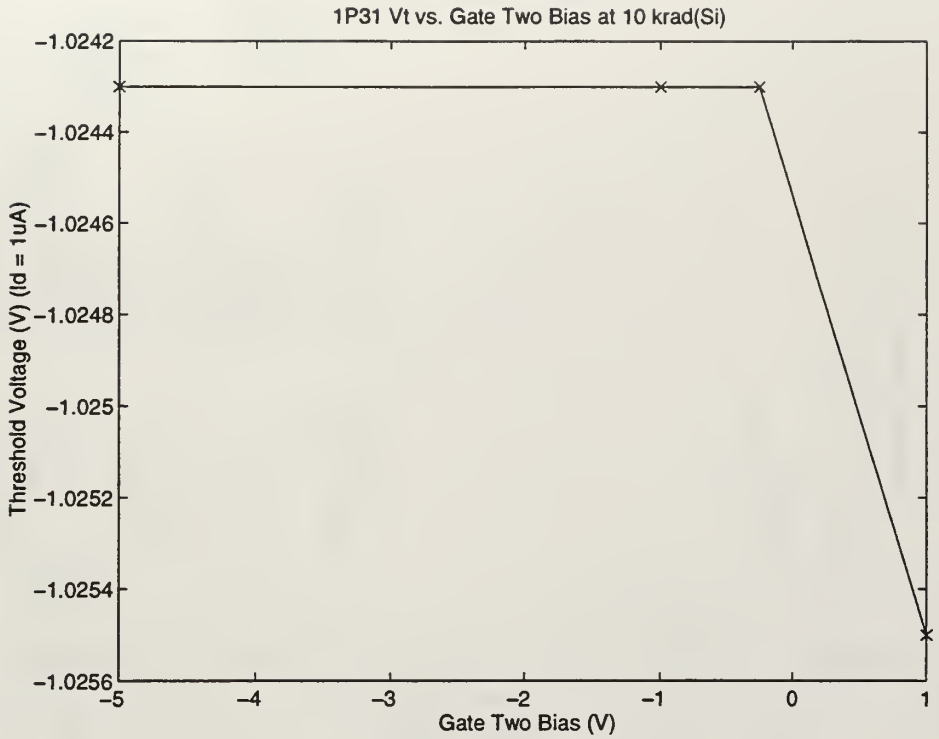


Figure C.140.

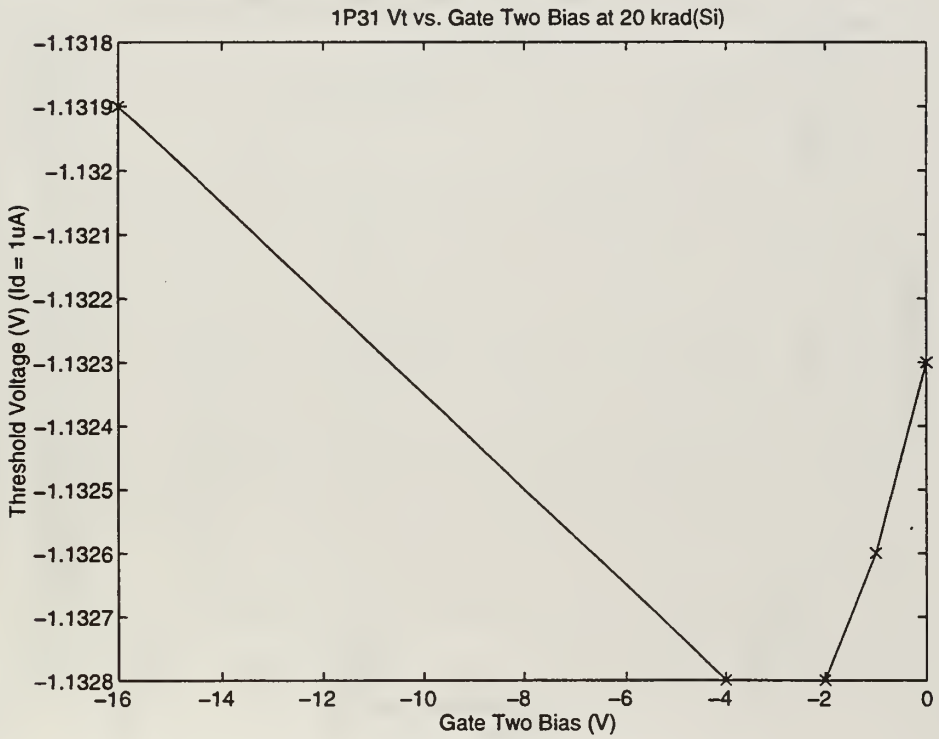


Figure C.141.

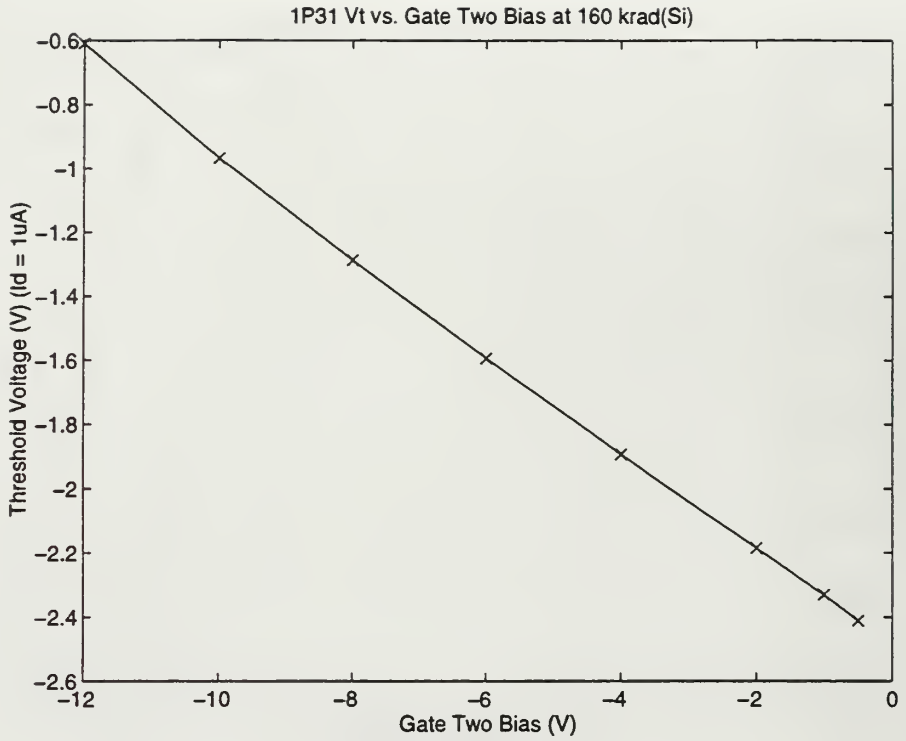


Figure C.142.

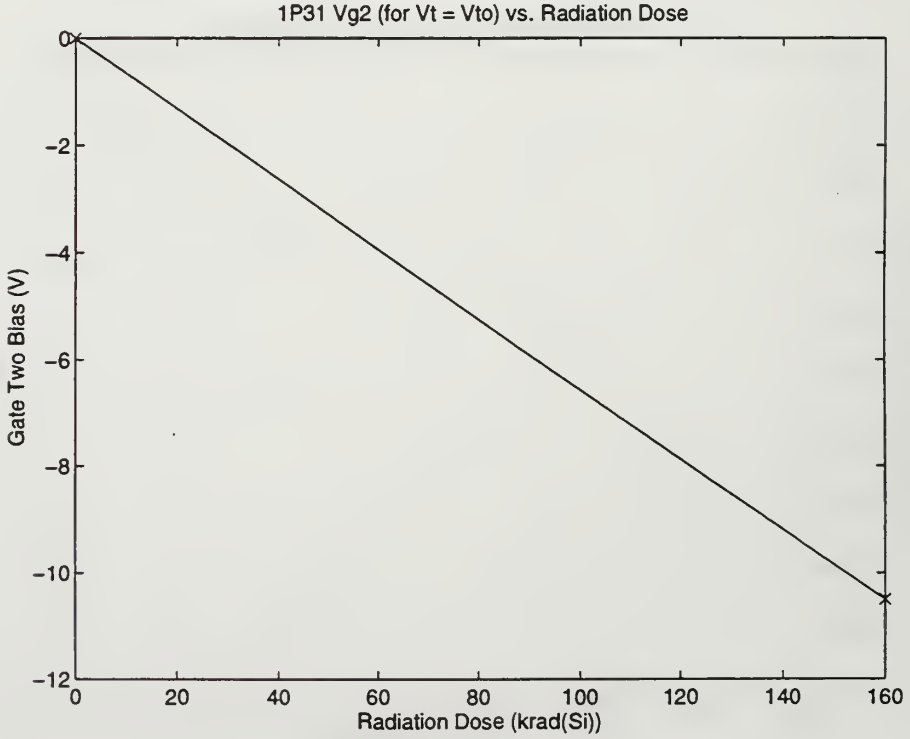


Figure C.143.

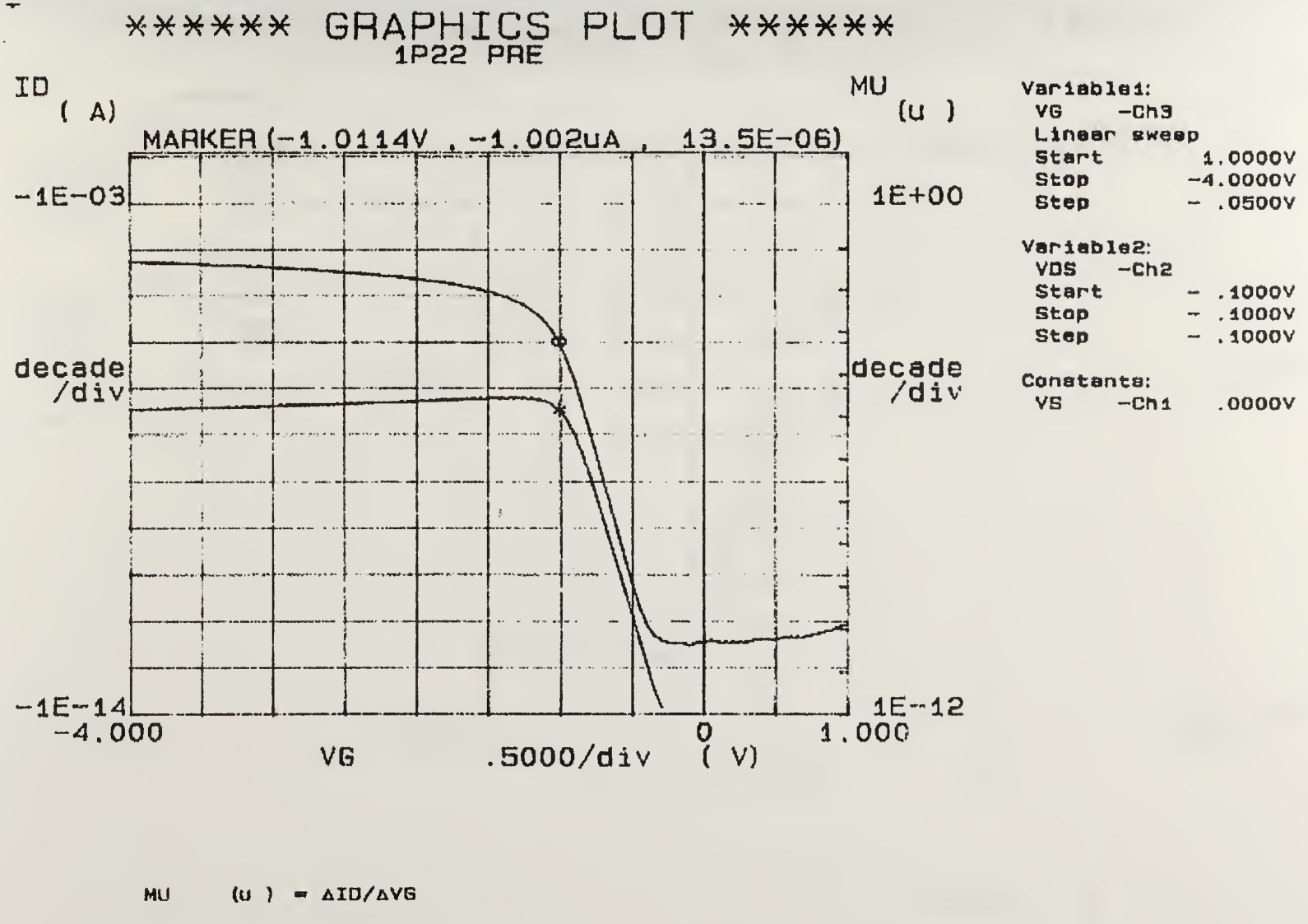

****** GRAPHICS PLOT ******
1P22 PRE
ID
(A)
MU
(u)
MARKER (-1.0114V , -1.002uA , 13.5E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.144.

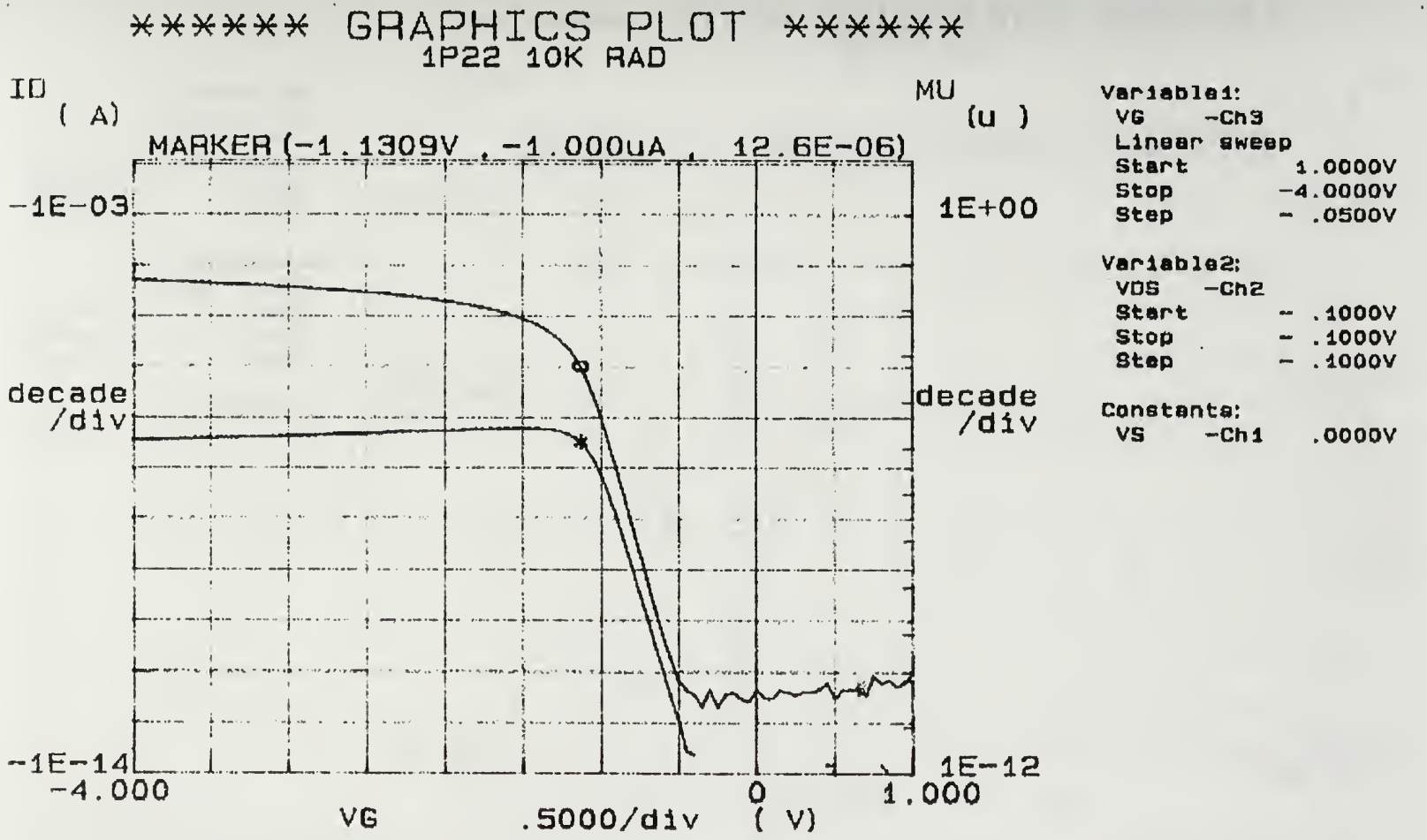

****** GRAPHICS PLOT ******
1P22 10K RAD
ID
(A)
MU
(u)
MARKER (-1.1309V , -1.000uA , 12.6E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.145.

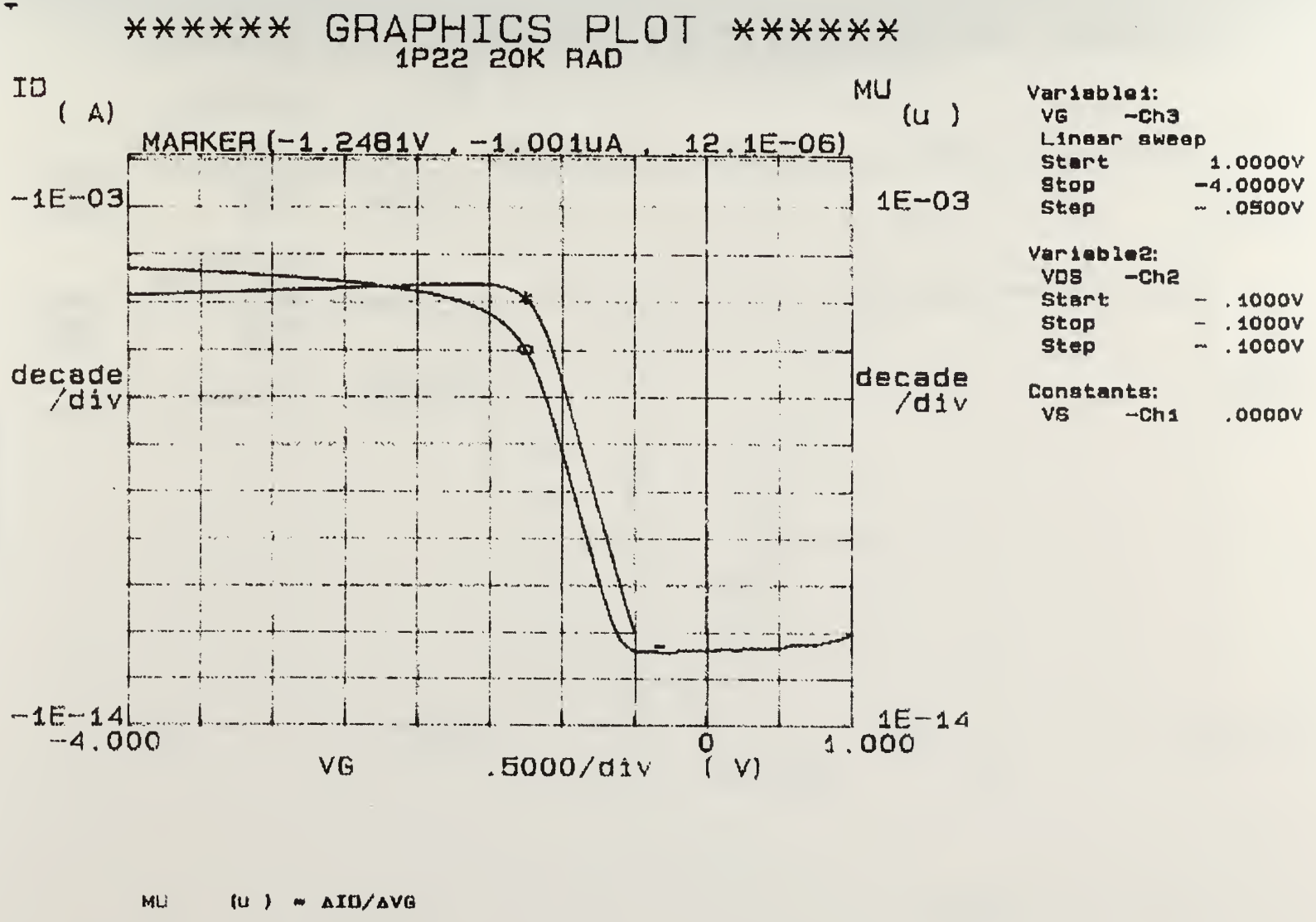
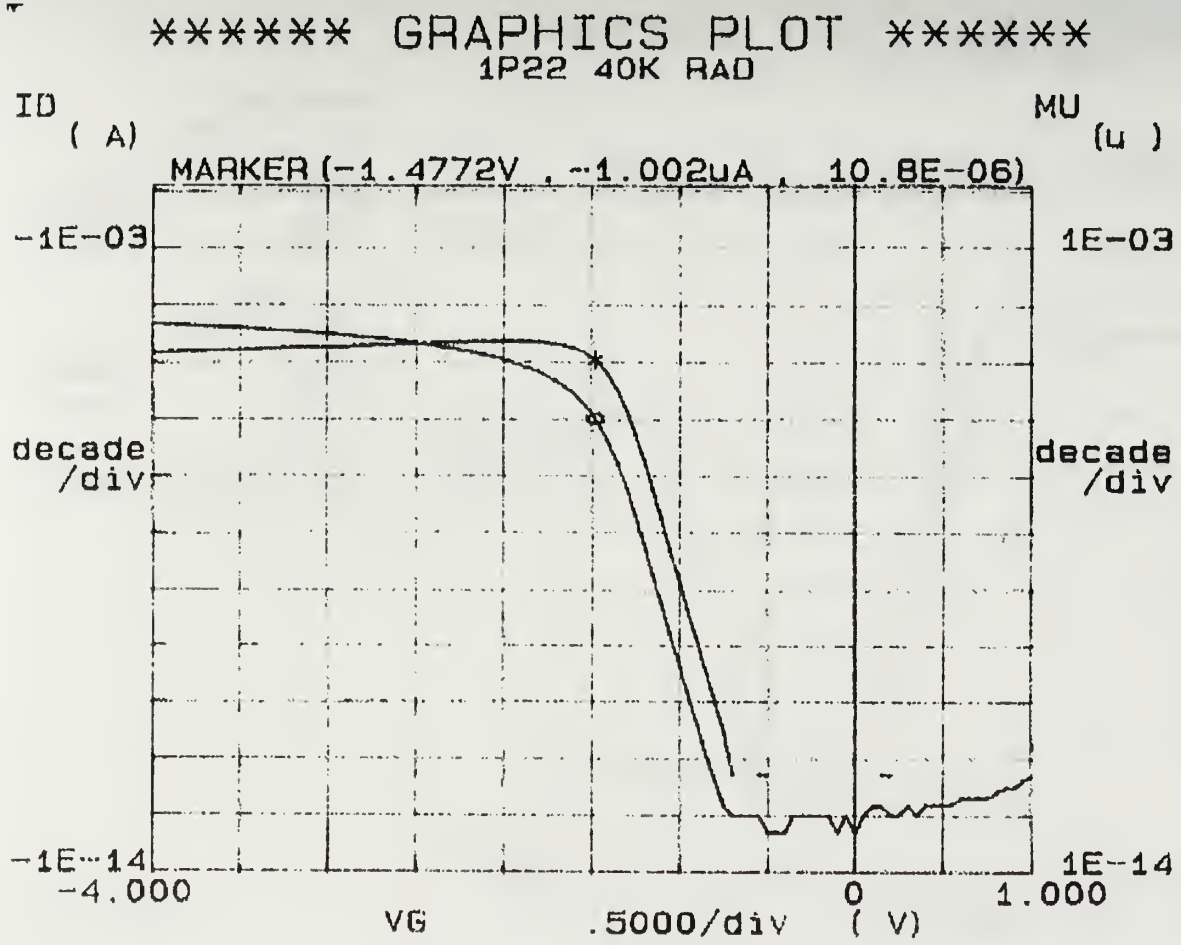

****** GRAPHICS PLOT ******
1P22 20K RAD
ID
(A)
MU
(u)
MARKER (-1.2481V , -1.001uA , 12.1E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.146.



Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V

Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V

Constants:
VS -Ch1 .0000V

Figure C.147.

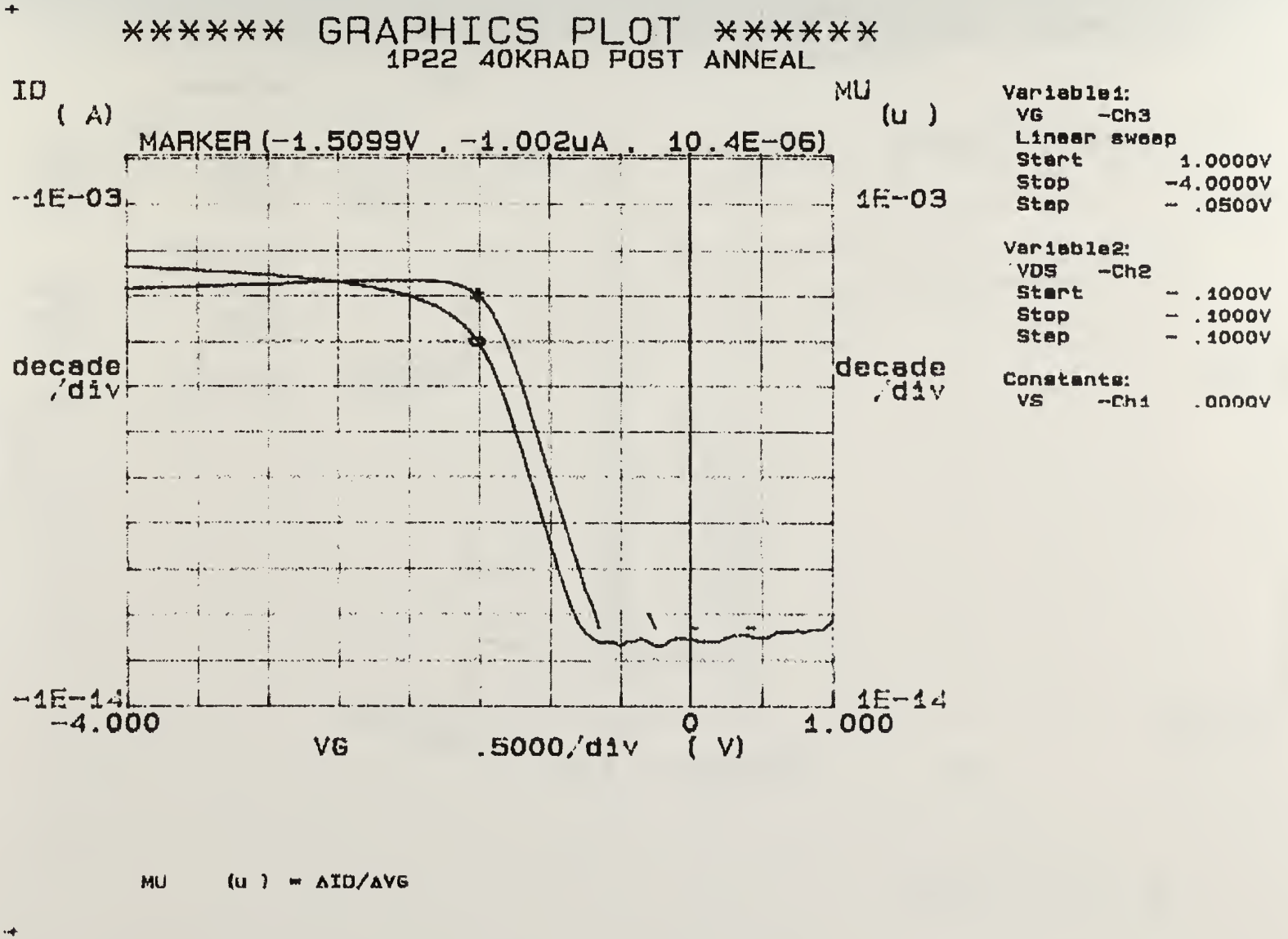

****** GRAPHICS PLOT ******
1P22 40KRAD POST ANNEAL
ID
(A)
MU
(u)
MARKER (-1.5099V , -1.002uA , 10.4E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = AID/AVG

Figure C.148.

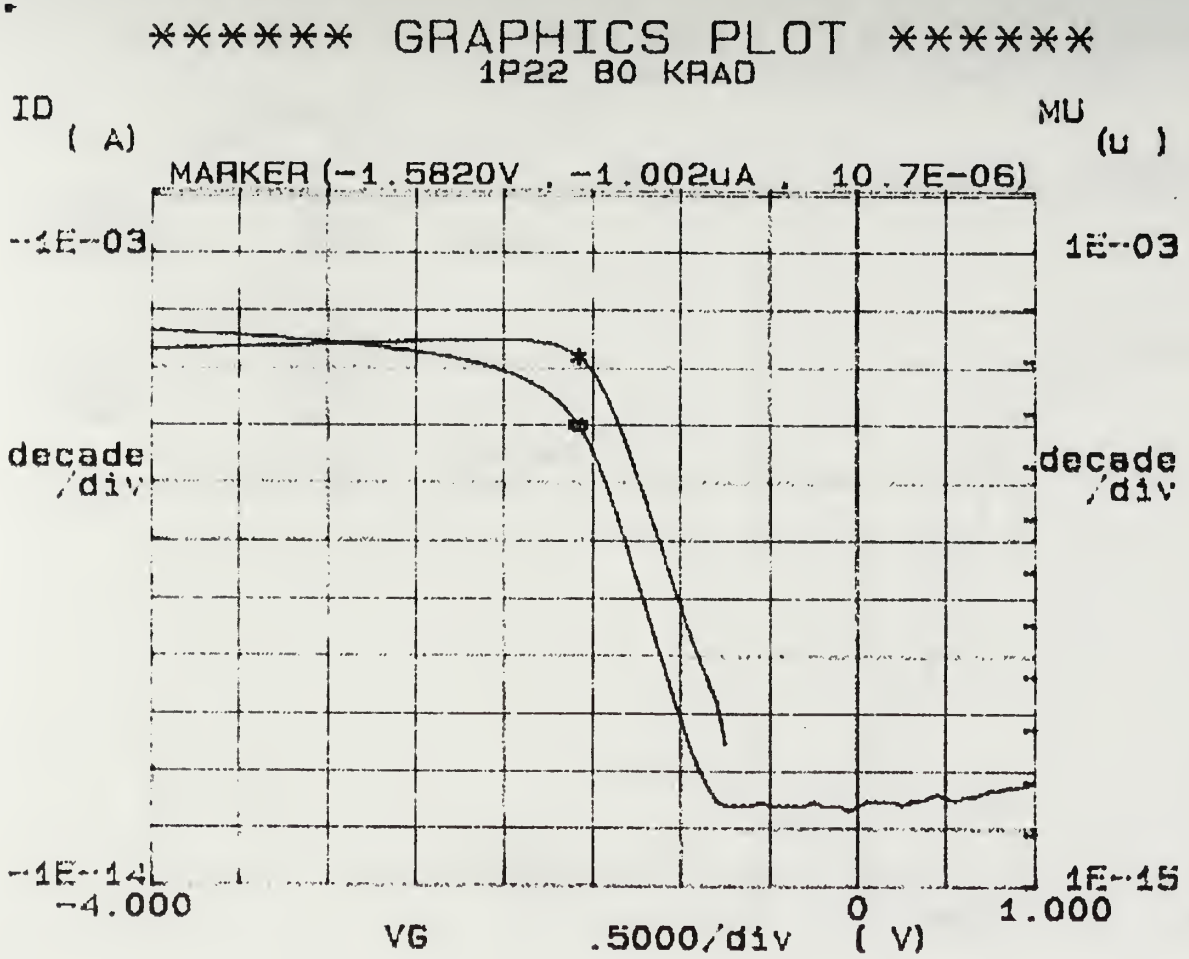

****** GRAPHICS PLOT ******
1P22 80 KRAD
ID
(A)
MU
(u)
MARKER (-1.5820V , -1.002uA , 10.7E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-15
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.149.

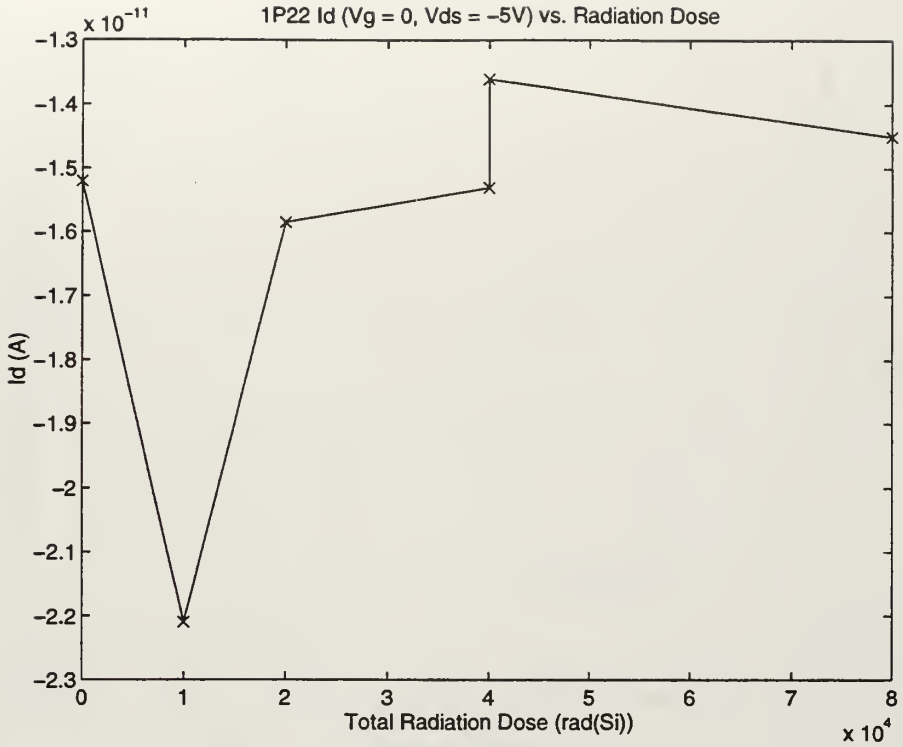


Figure C.150.

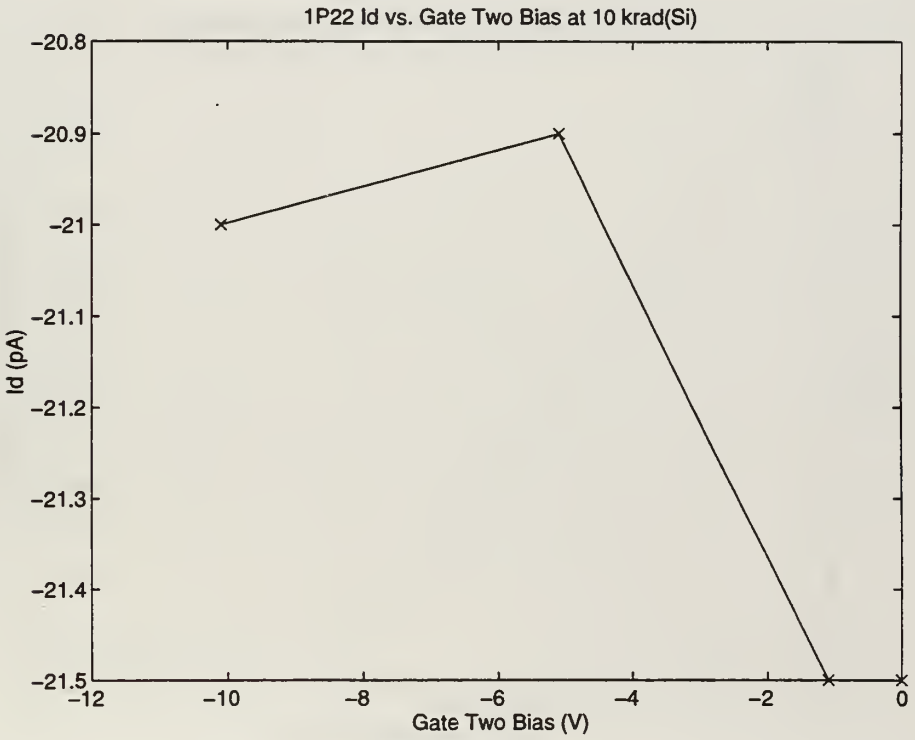


Figure C.151.

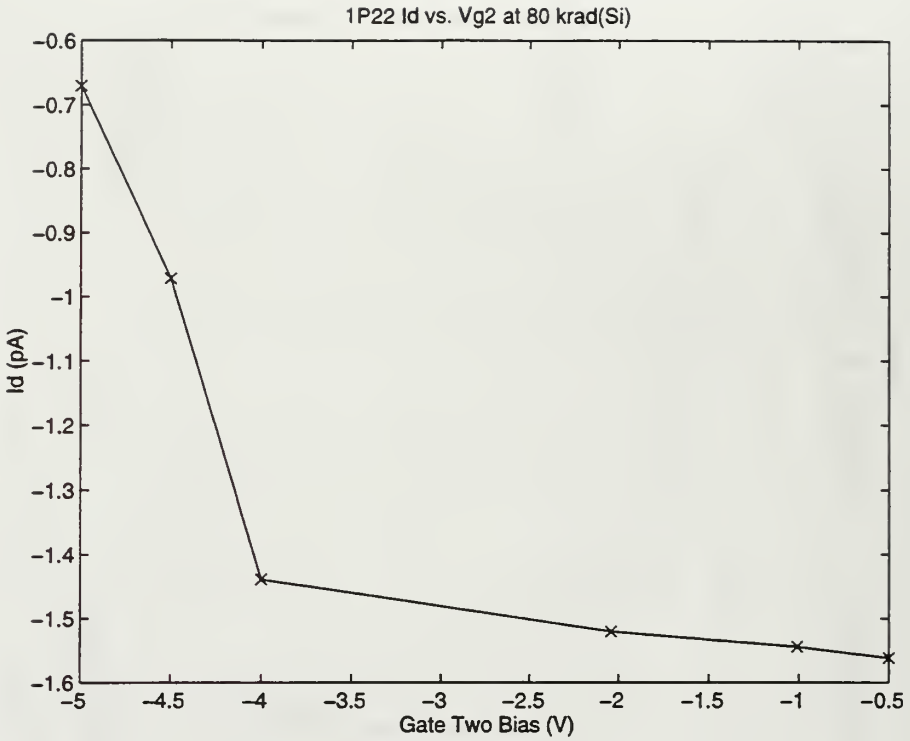


Figure C.152.

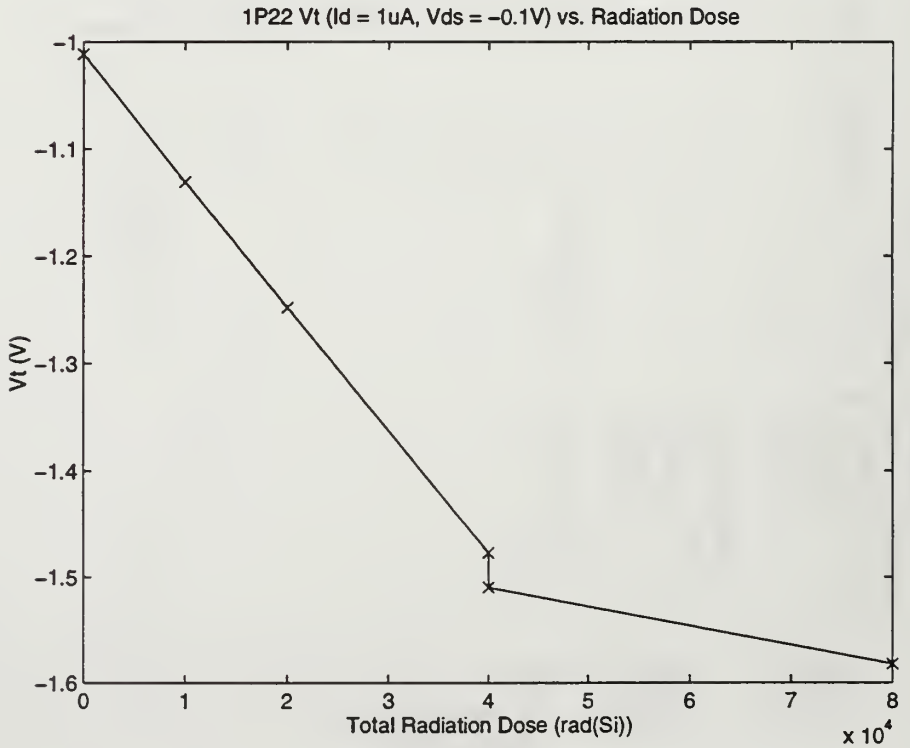


Figure C.153.

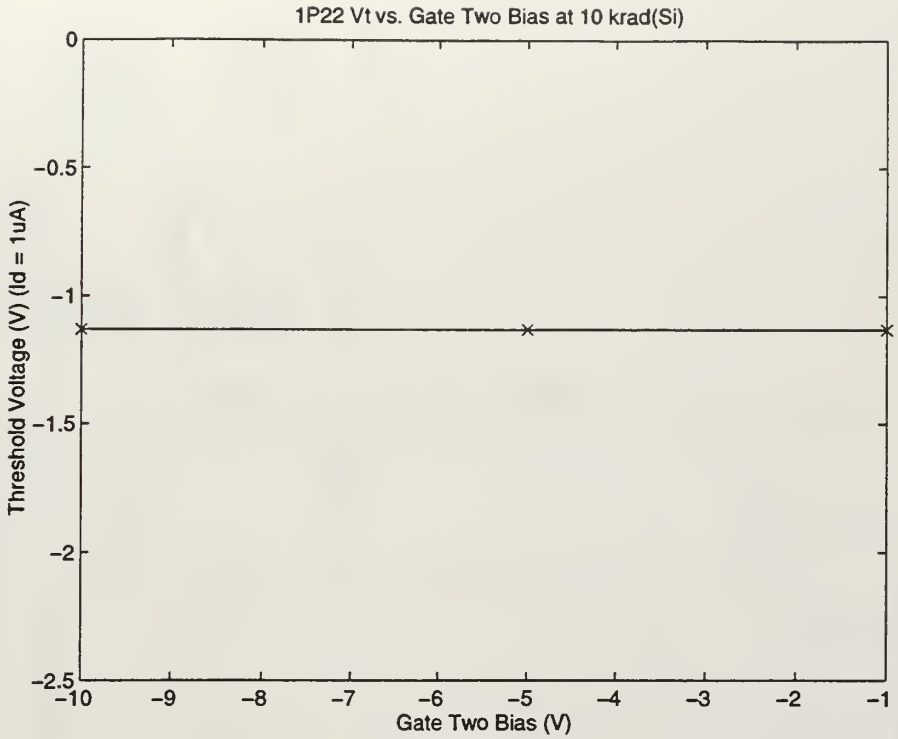


Figure C.154.

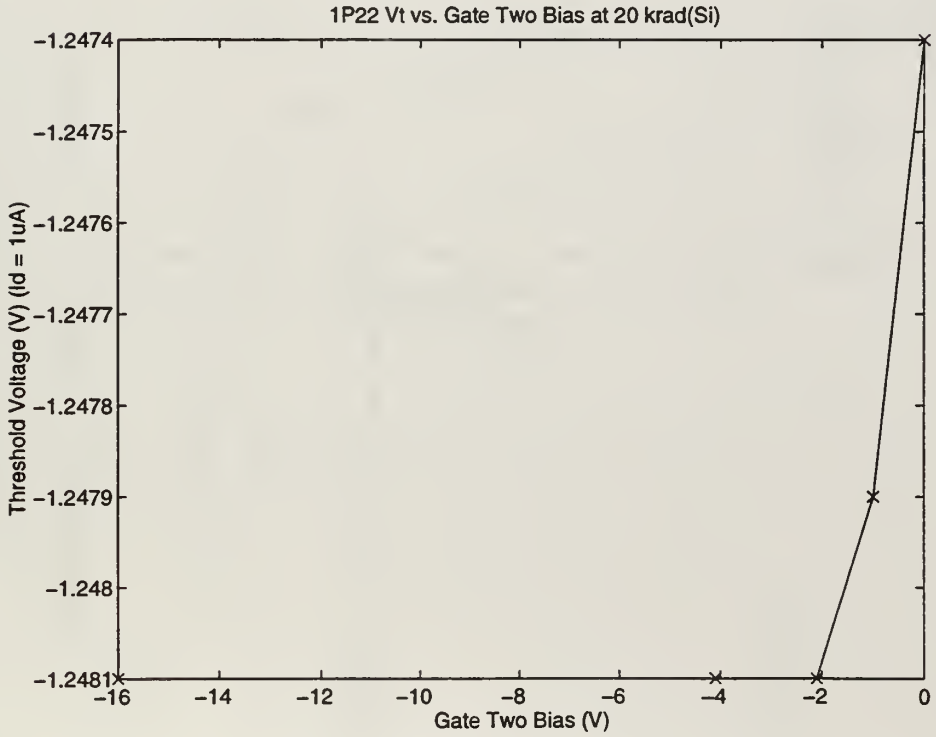
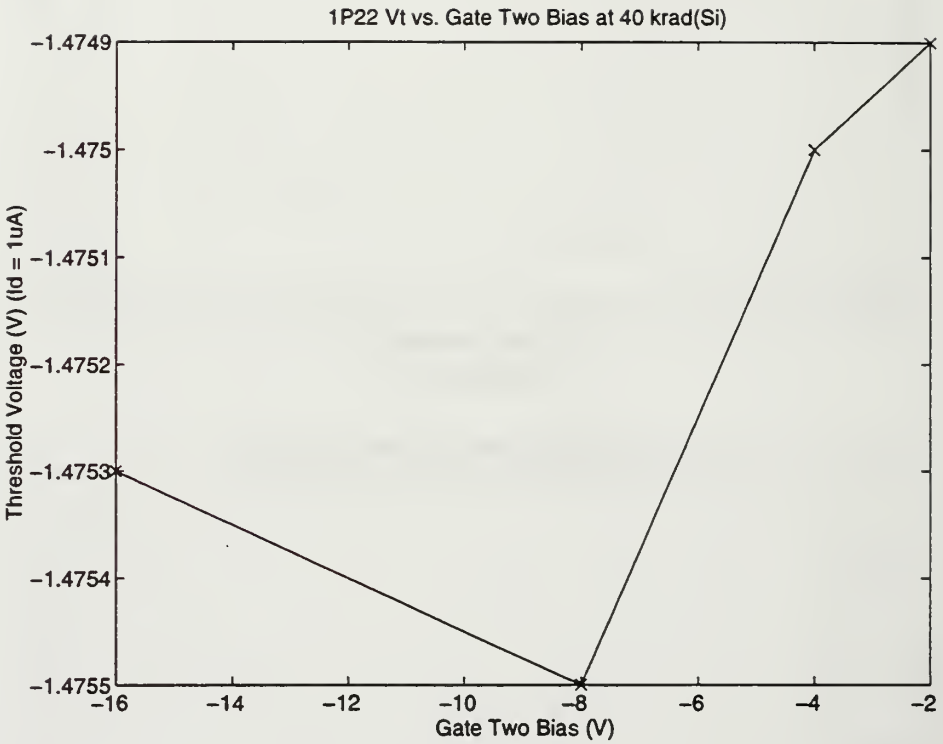


Figure C.155.


1P22 Vt vs. Gate Two Bias at 40 krad(Si)
Threshold Voltage (V) (Id = 1uA)
-1.4749
-1.475
-1.4751
-1.4752
-1.4753
-1.4754
-1.4755
-16
-14
-12
-10
-8
-6
-4
-2
Gate Two Bias (V)
Figure C.156.

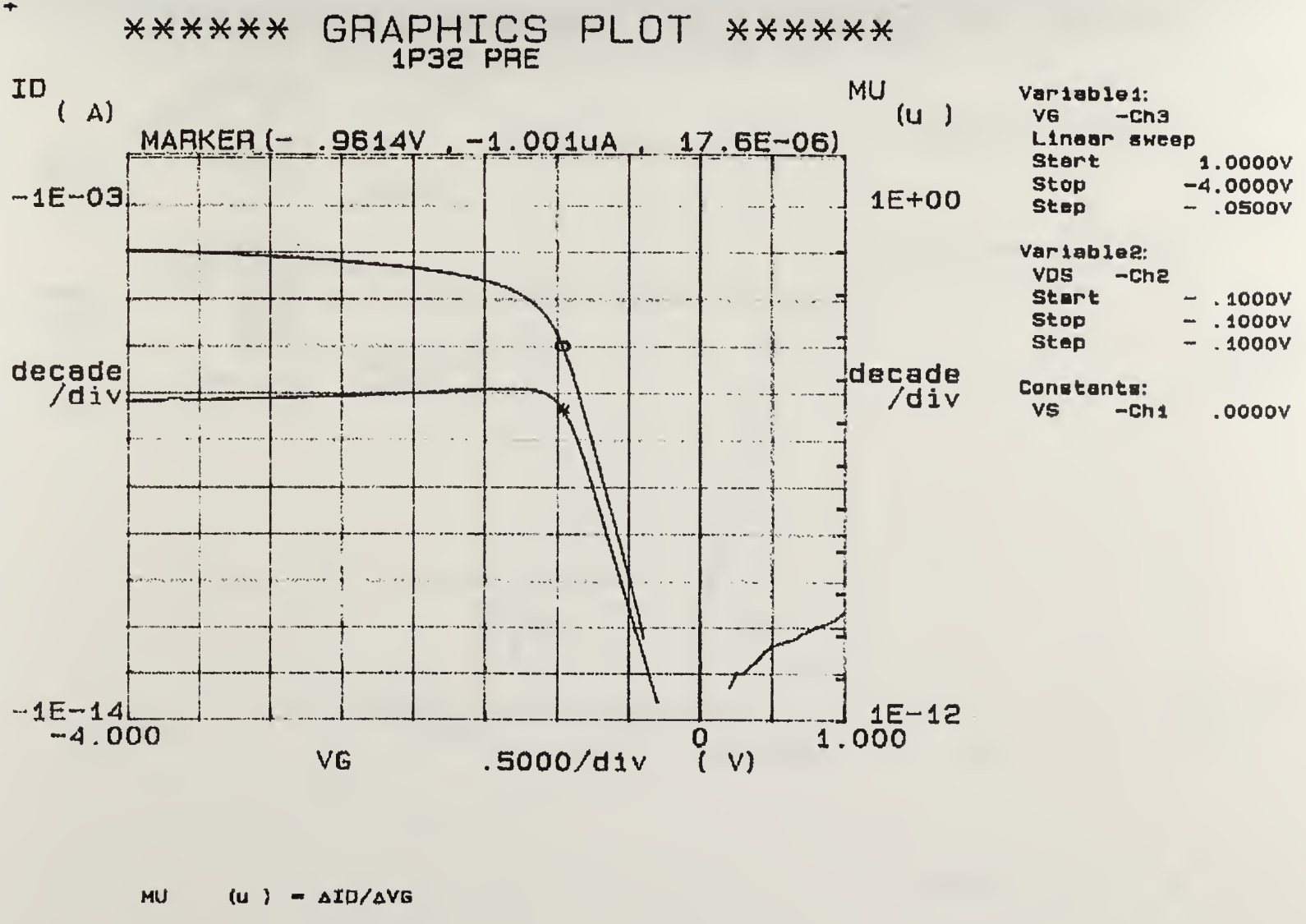

****** GRAPHICS PLOT ******
1P32 PRE
ID
(A)
MU
(u)
MARKER (- .9614V , -1.001uA , 17.6E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.157.

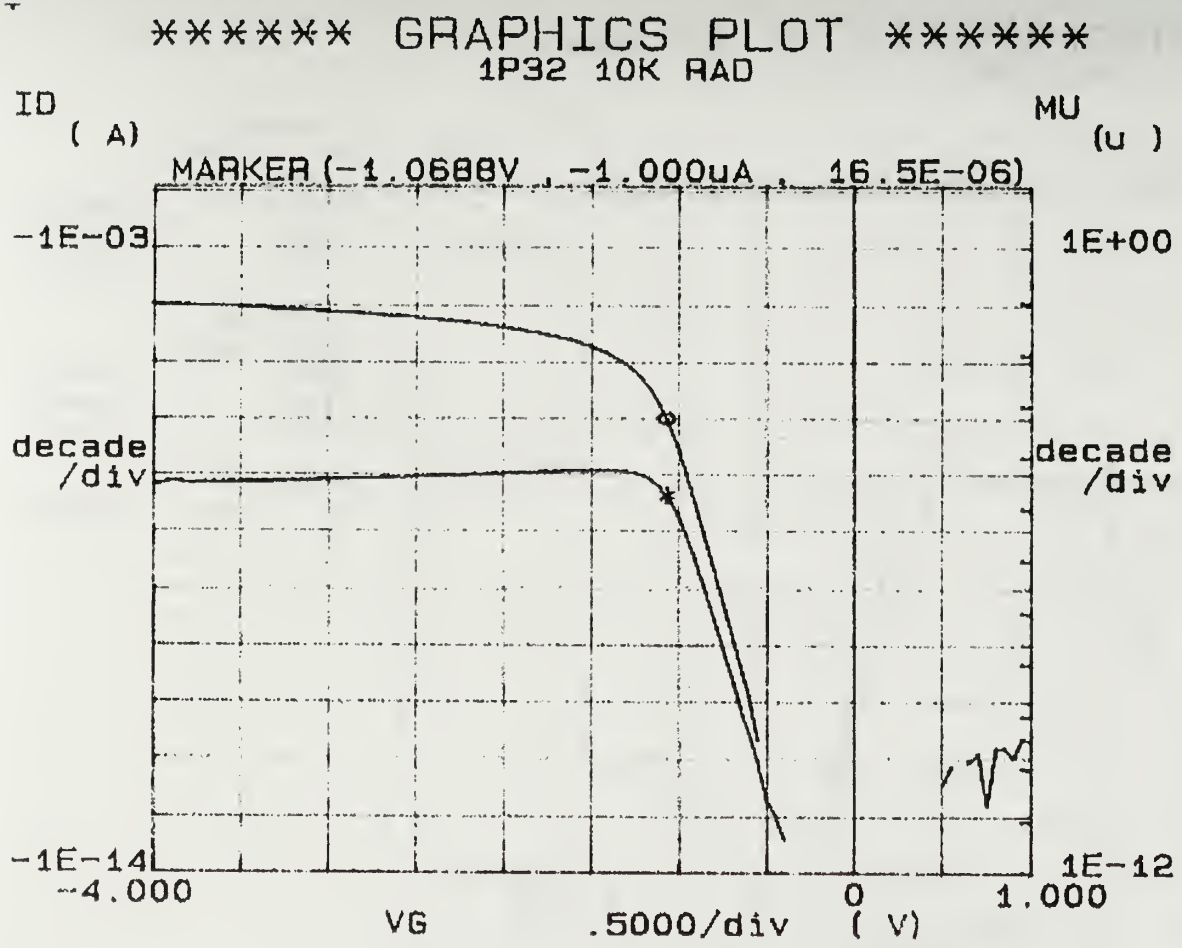

****** GRAPHICS PLOT ******
1P32 10K RAD
ID
(A)
MU
(u)
MARKER (-1.0688V , -1.000uA , 16.5E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.158.

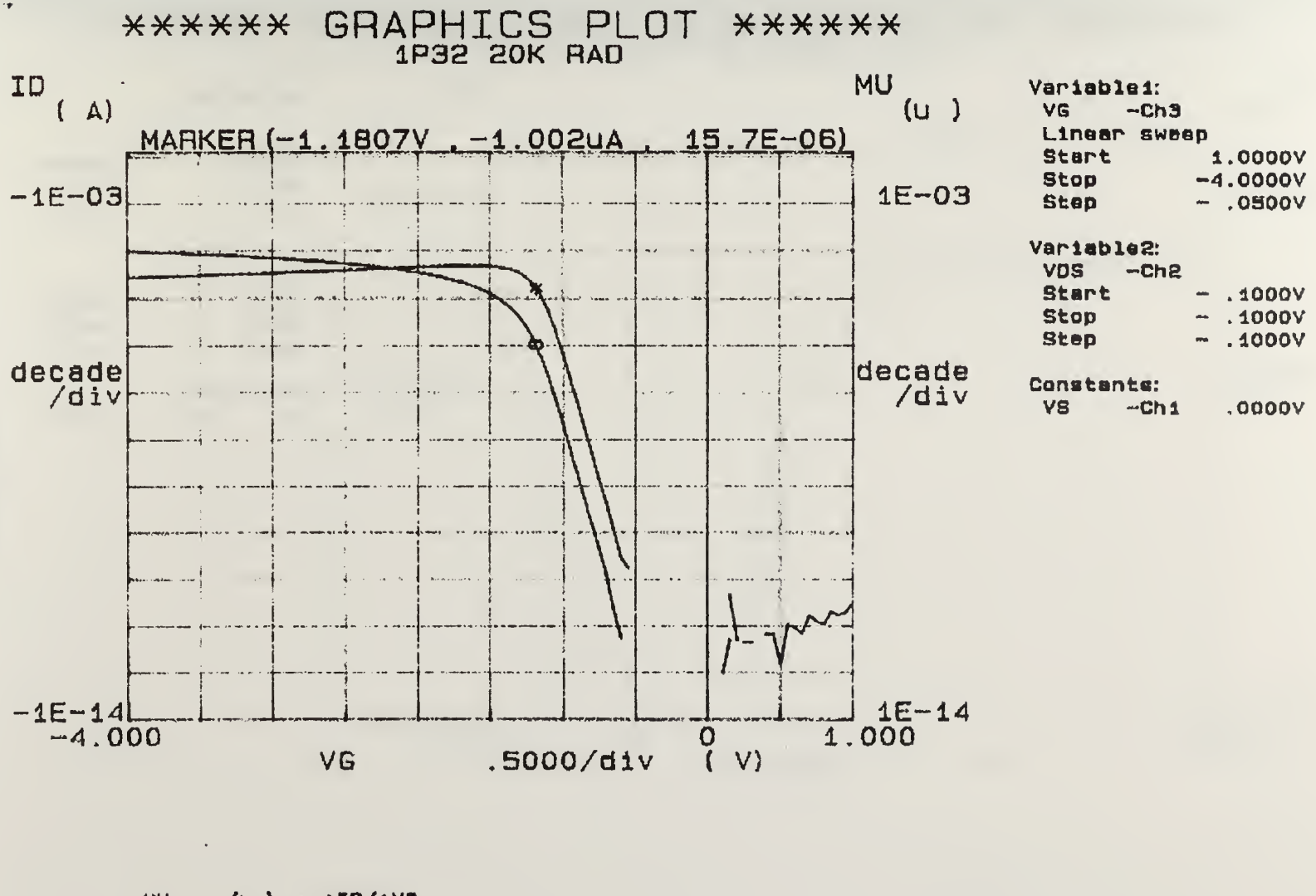

****** GRAPHICS PLOT ******
1P32 20K RAD
ID
(A)
MU
(u)
MARKER (-1.1807V , -1.002uA , 15.7E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.159.

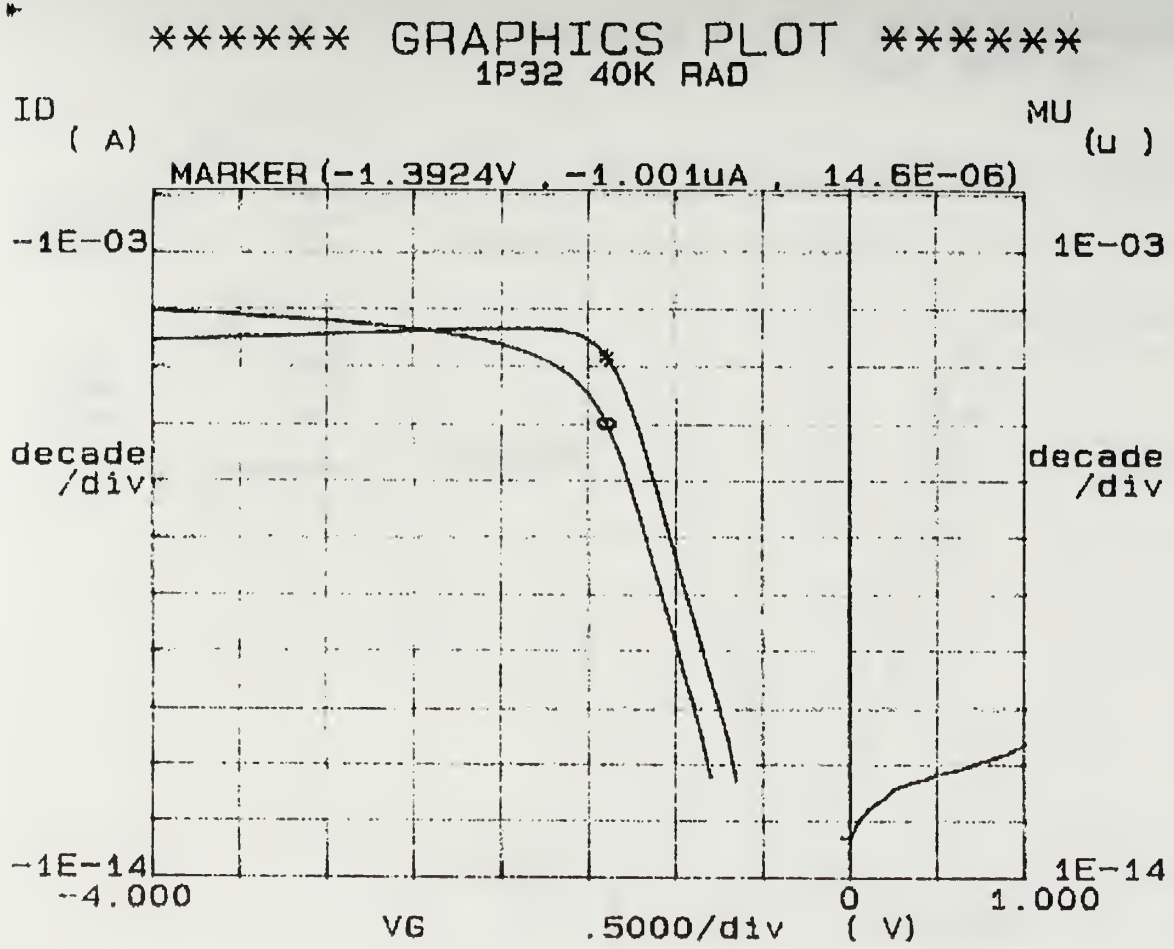

****** GRAPHICS PLOT ******
1P32 40K RAD
ID
(A)
MU
(u)
MARKER (-1.3924V , -1.001uA , 14.6E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.160.

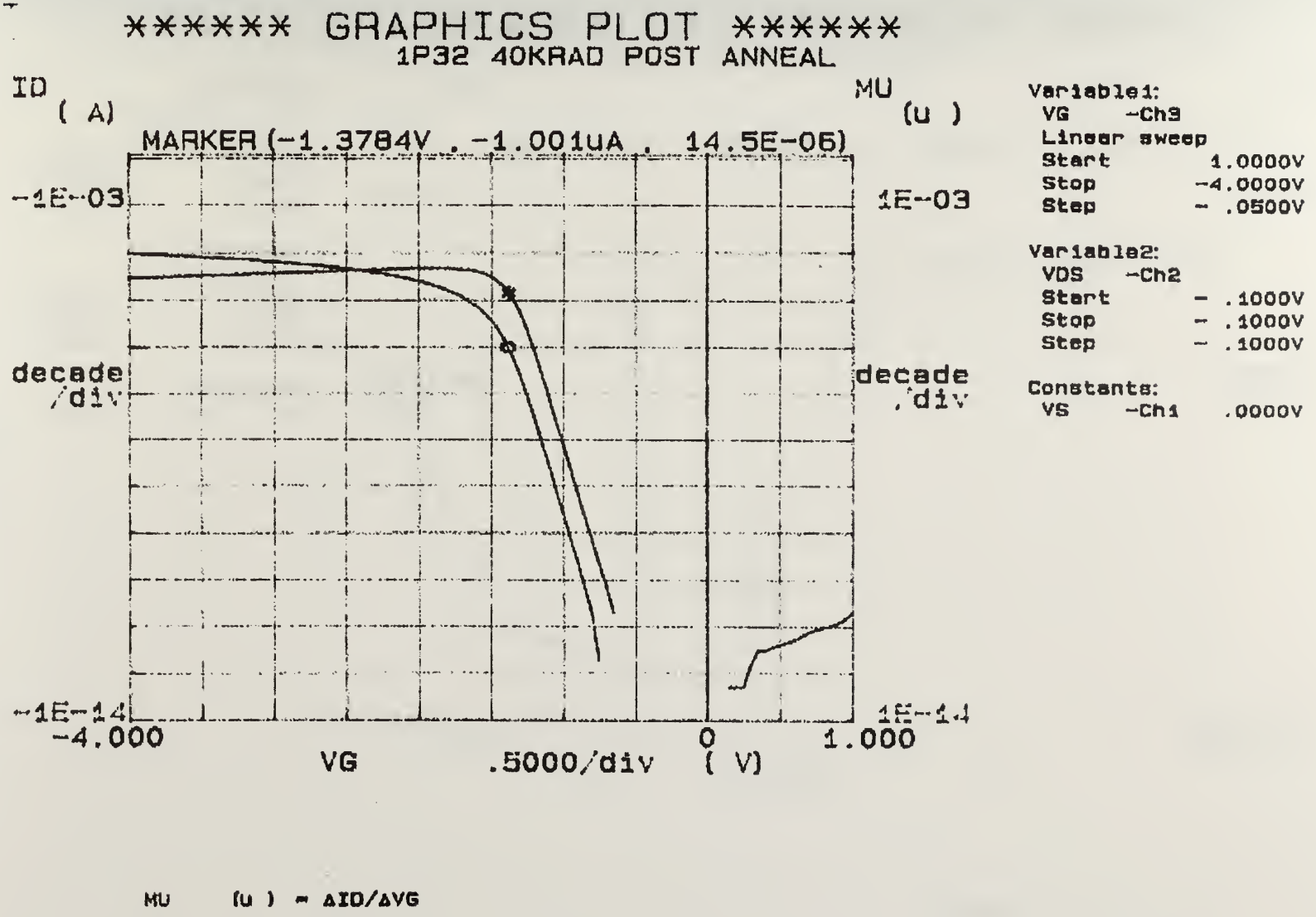

****** GRAPHICS PLOT ******
1P32 40KRAD POST ANNEAL
ID
(A)
MU
(u)
MARKER (-1.3784V , -1.001uA , 14.5E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG .5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.161.

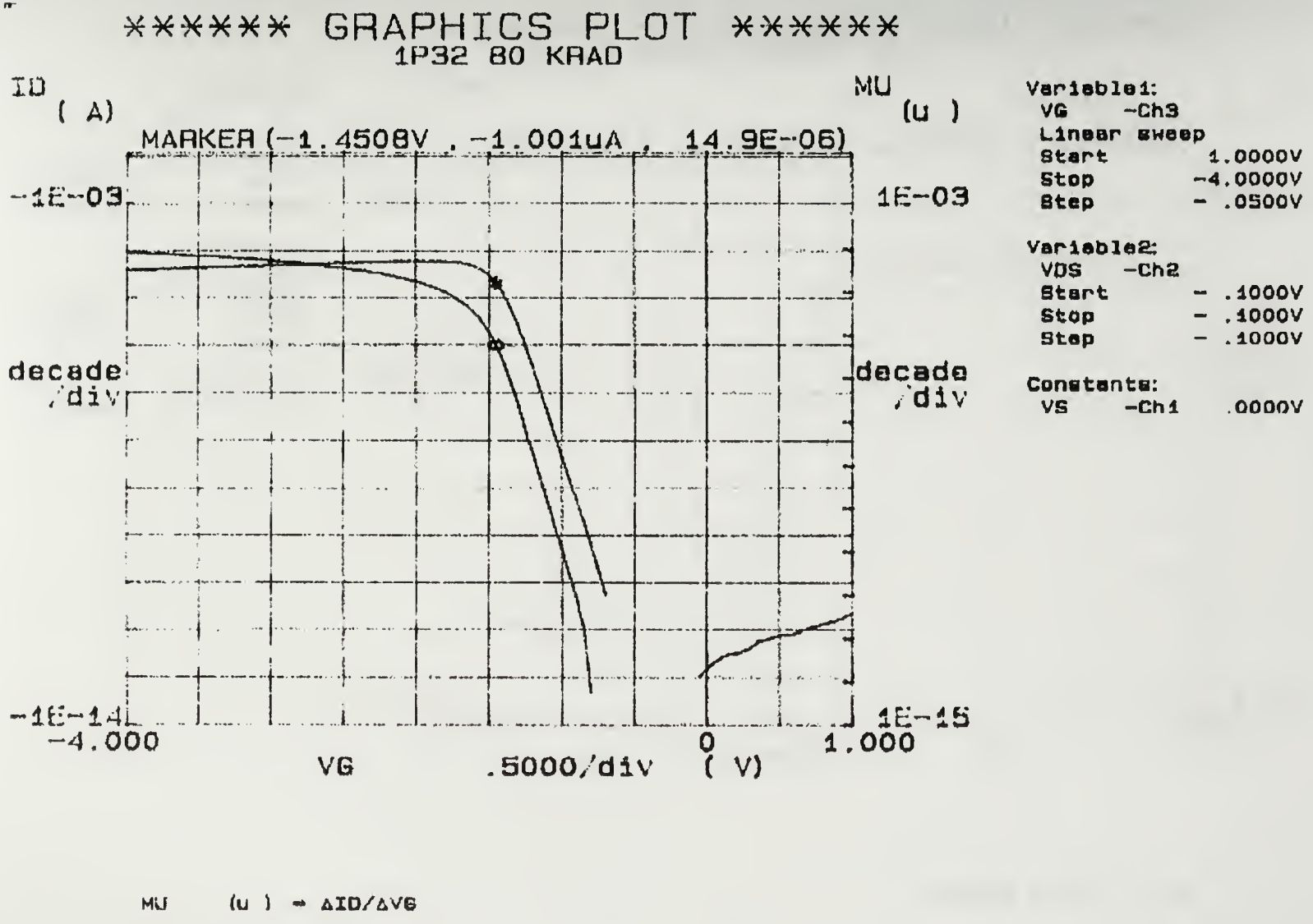

****** GRAPHICS PLOT ******
1P32 80 KRAD
ID
(A)
MU
(u)
MARKER (-1.4508V , -1.001uA , 14.9E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-15
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.162.

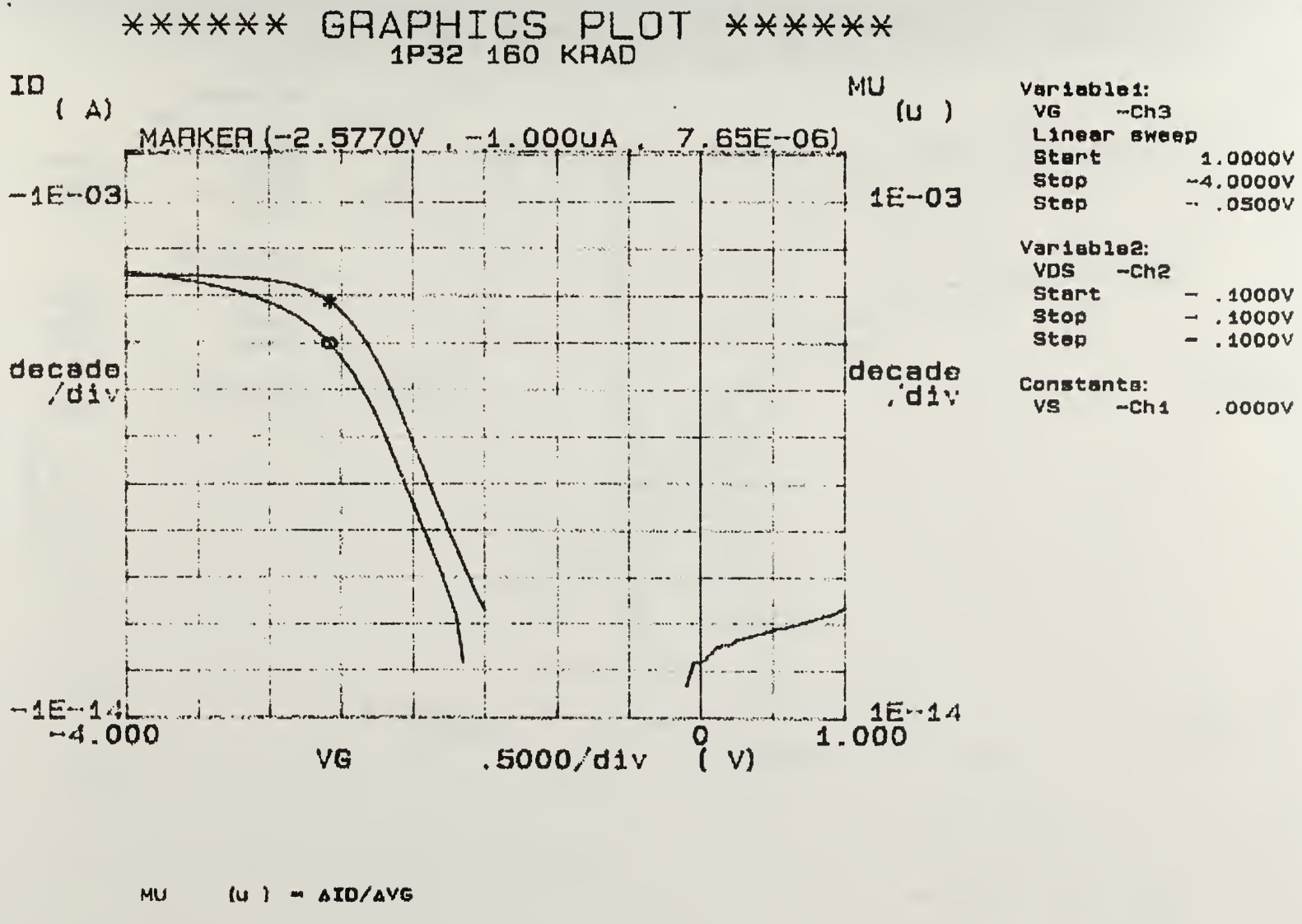

****** GRAPHICS PLOT ******
1P32 160 KRAD
ID
(A)
MU
(u)
MARKER (-2.5770V , -1.000uA , 7.65E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG .5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step -.0500V
Variable2:
VDS -Ch2
Start -.1000V
Stop -.1000V
Step -.1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.163.

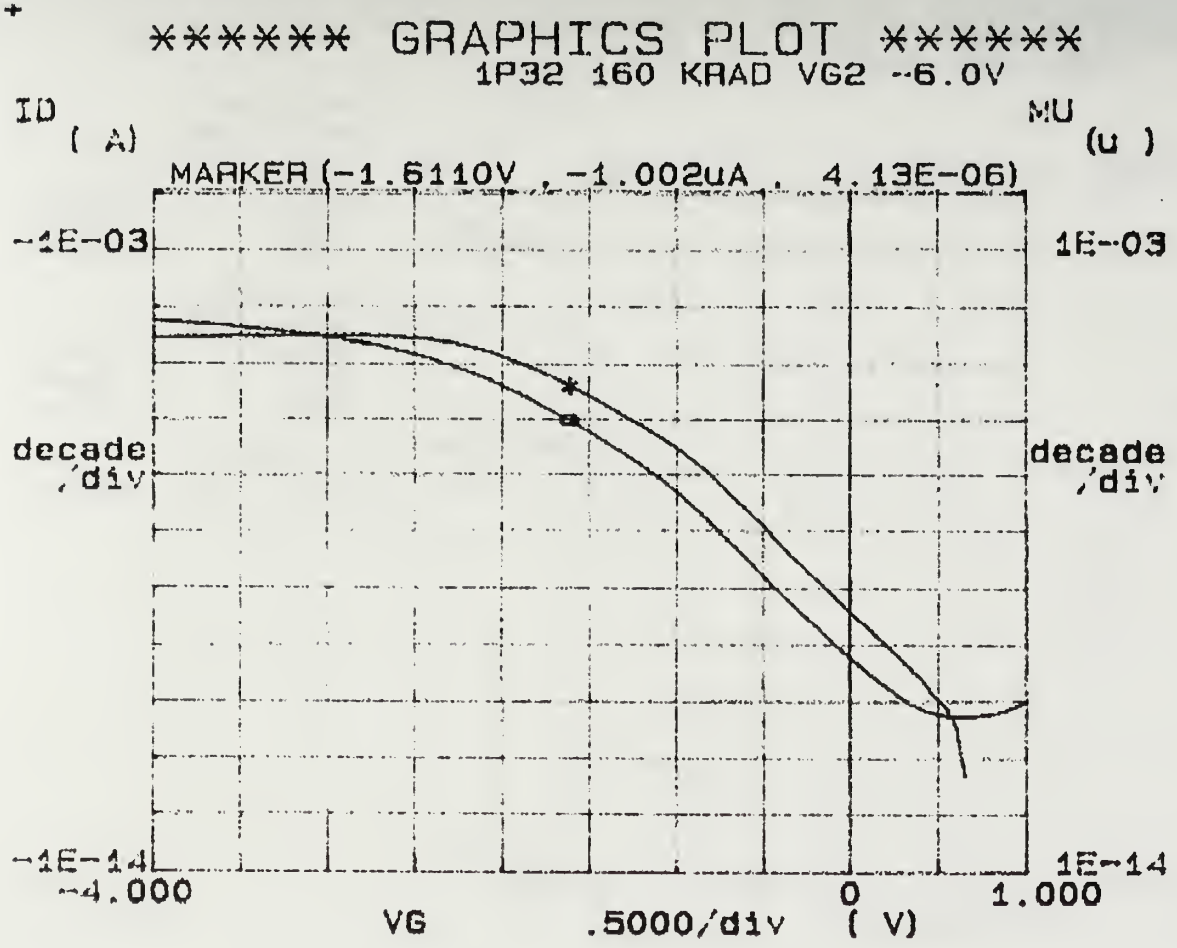

****** GRAPHICS PLOT ******
1P32 160 KRAD VG2 -6.0V
ID
(A)
MU
(u)
MARKER (-1.6110V , -1.002uA , 4.13E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step -.0500V
Variable2:
VDS -Ch2
Start -.1000V
Stop -.1000V
Step -.1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.164.

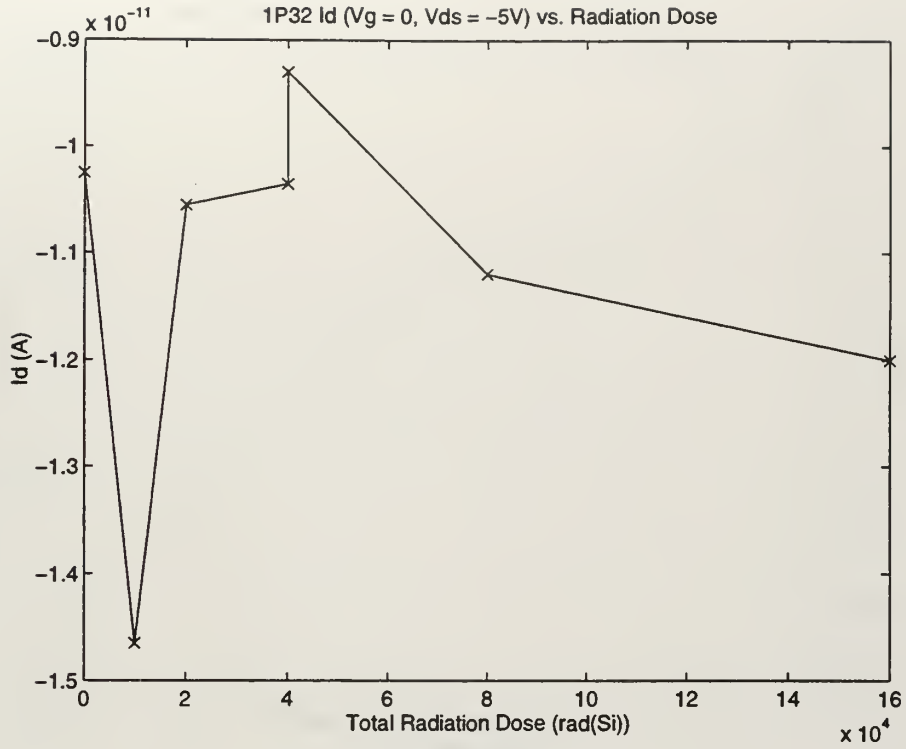


Figure C.165.

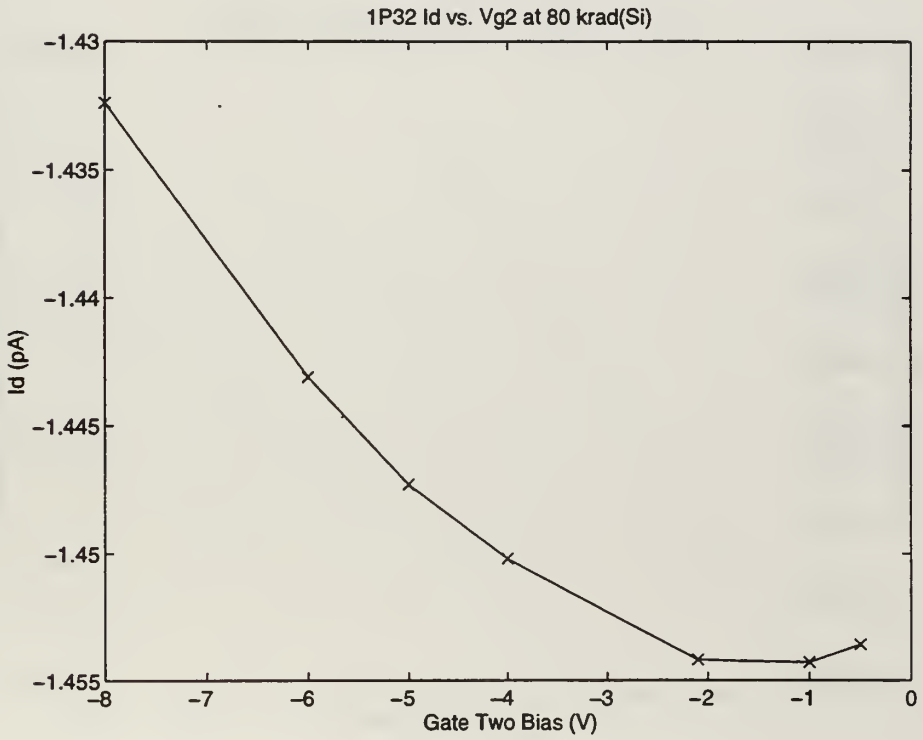


Figure C.166.

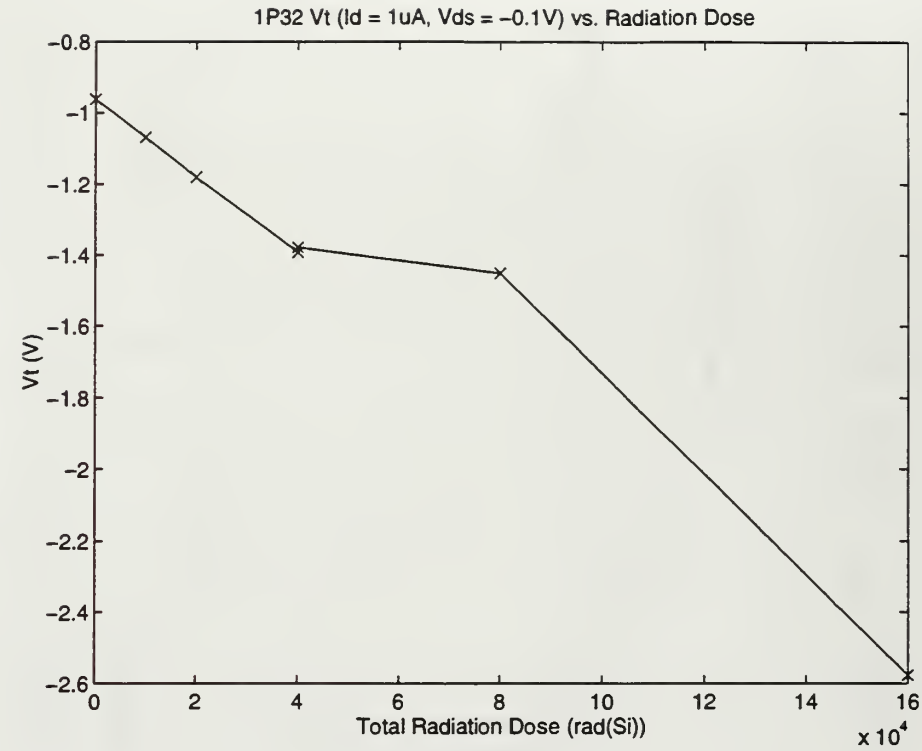


Figure C.167.

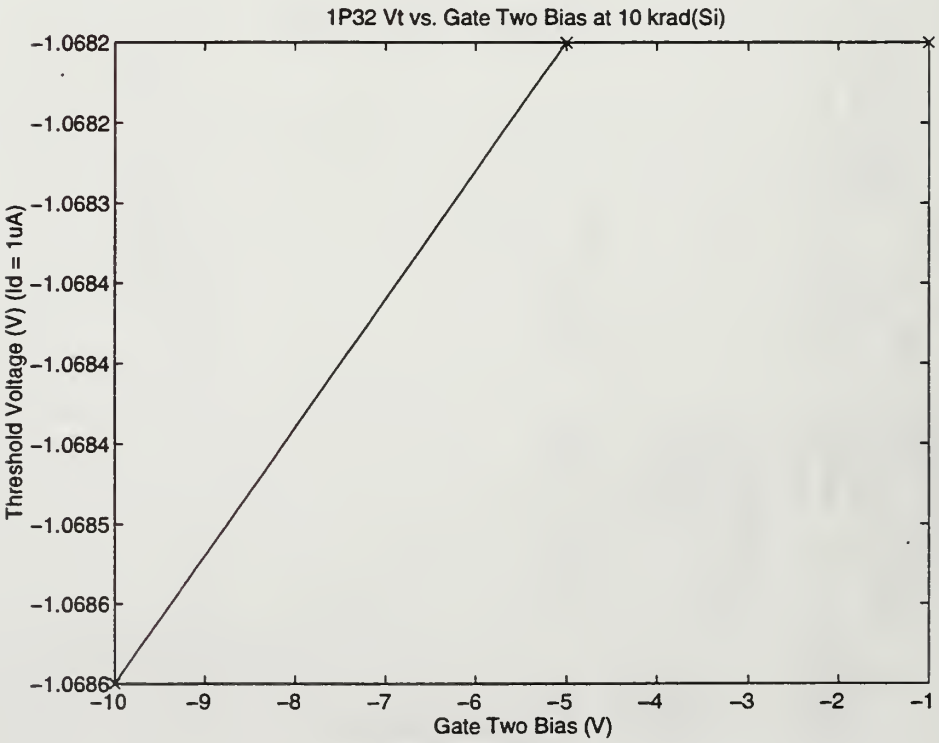


Figure C.168.

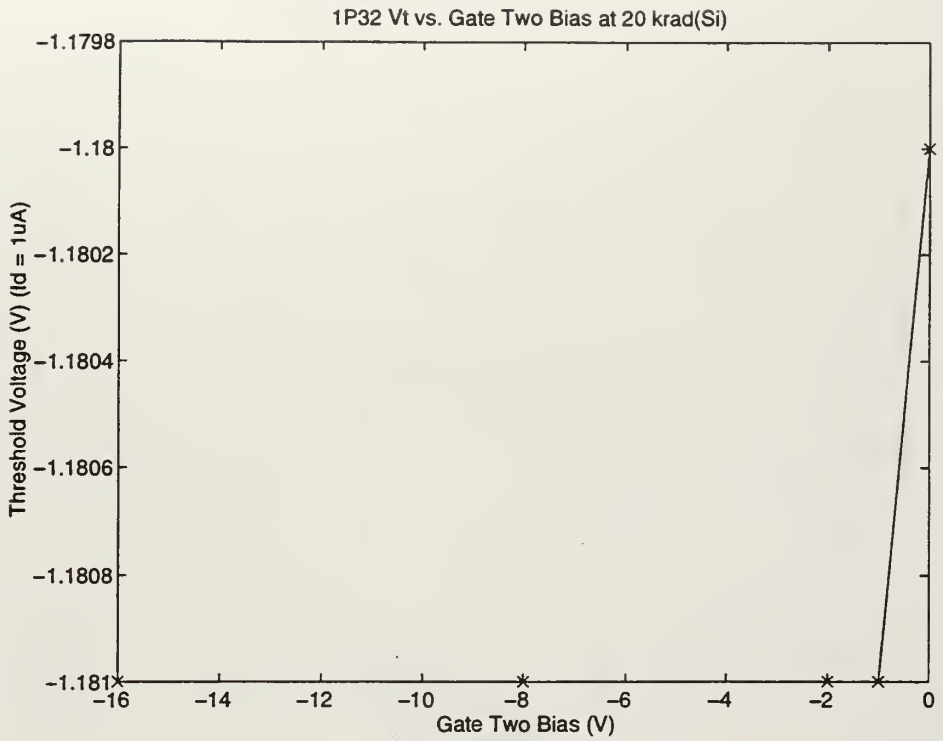


Figure C.169.

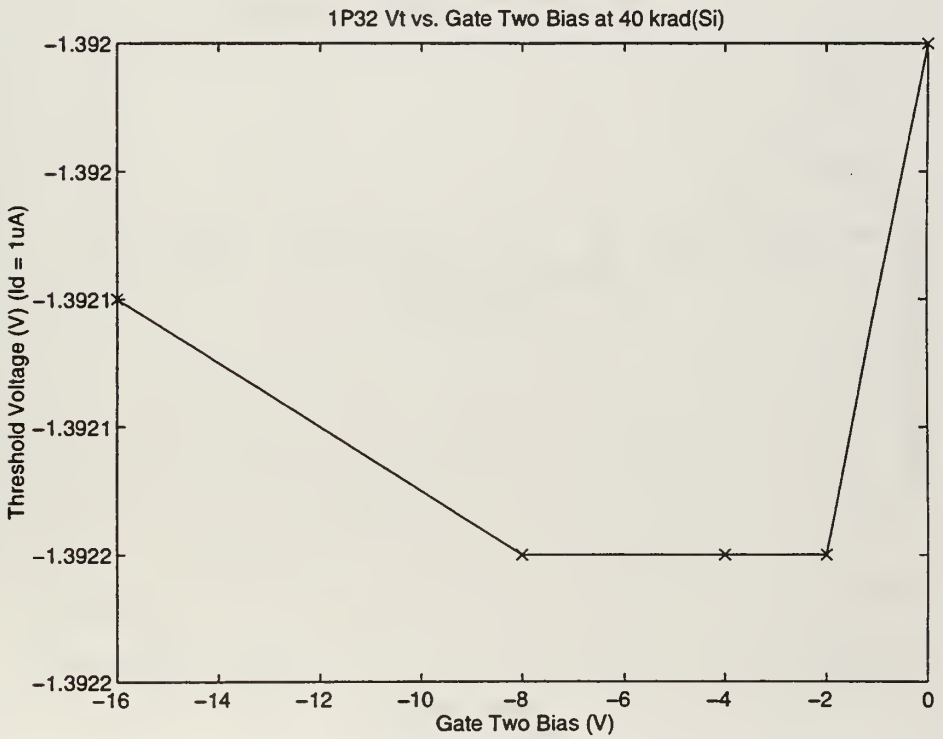


Figure C.170.

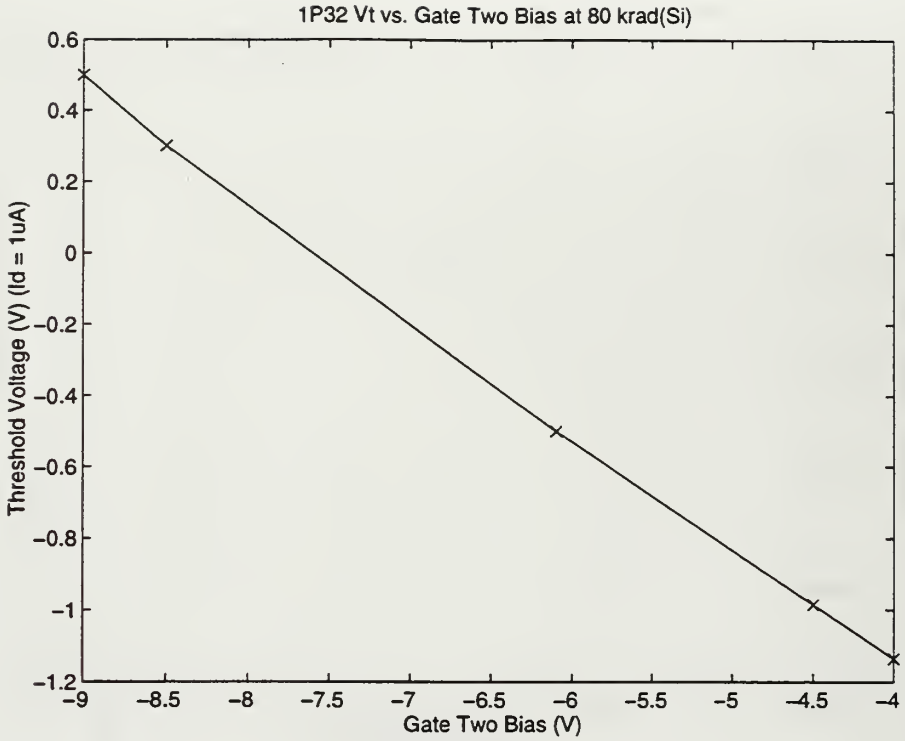


Figure C.171.

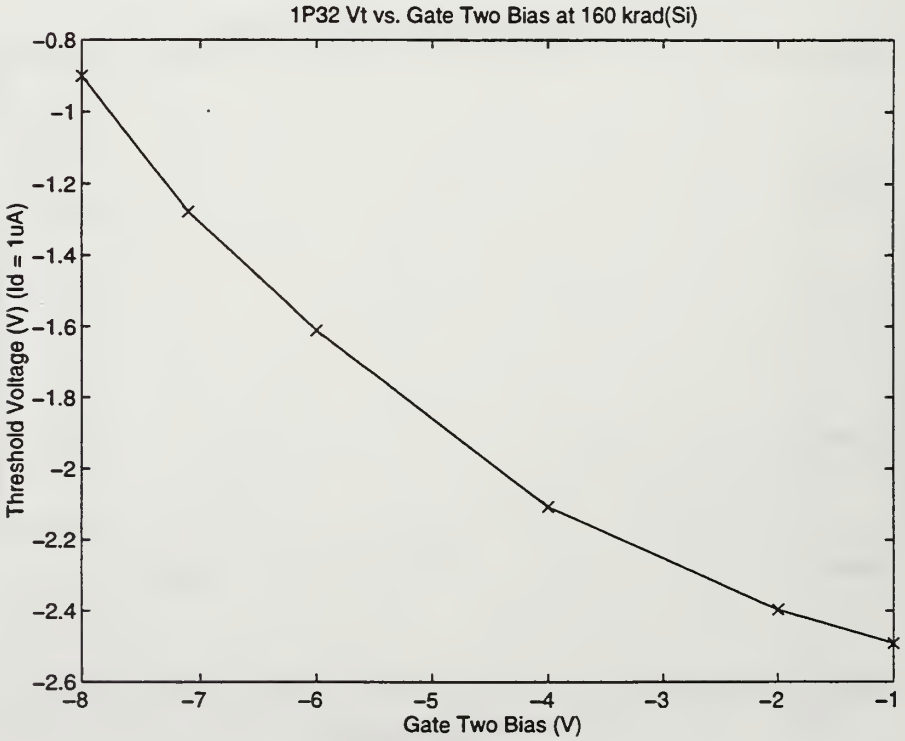


Figure C.172.

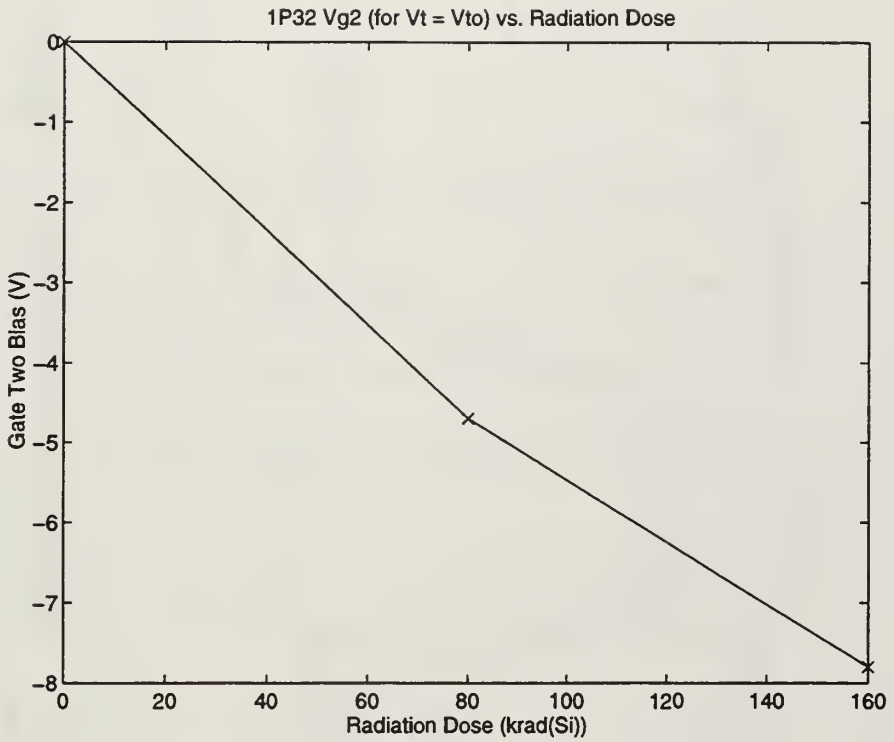
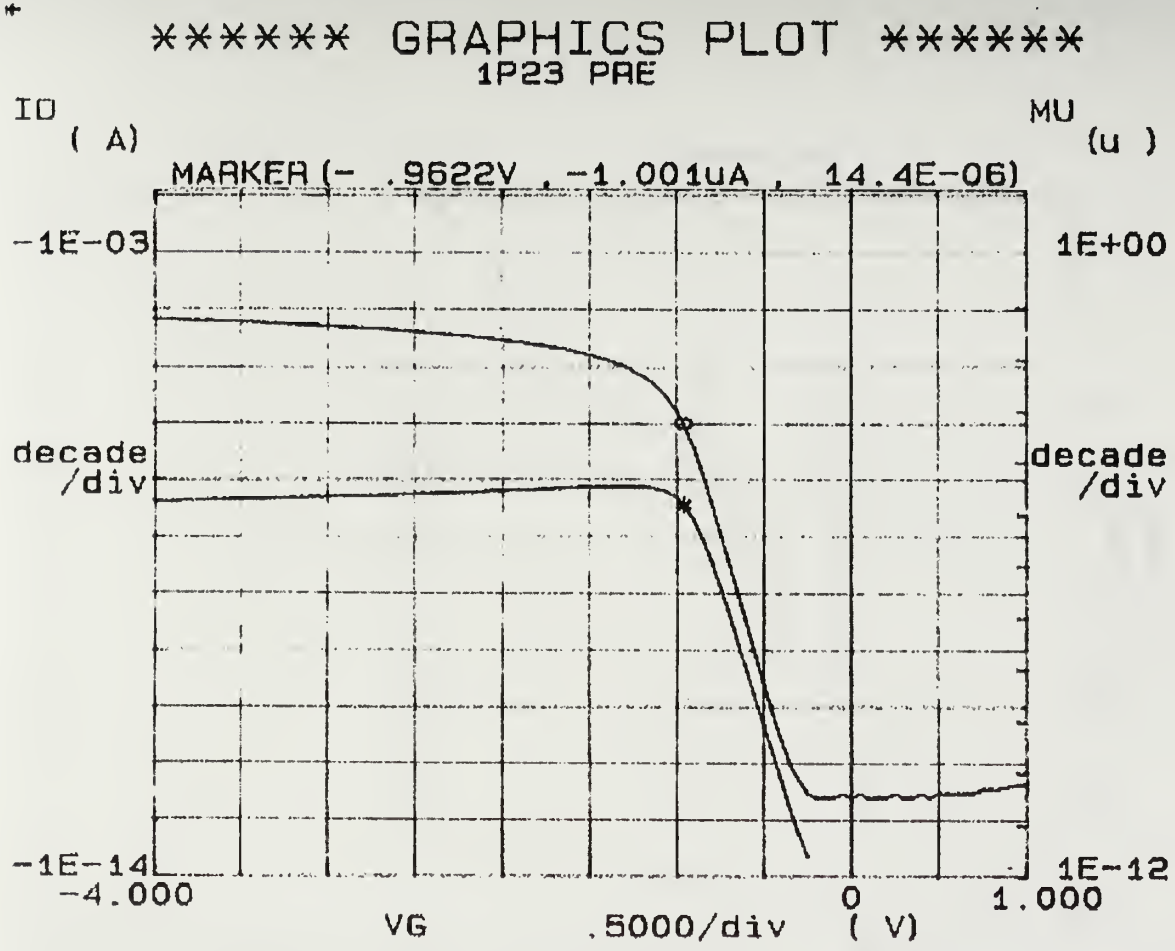

1P32 Vg2 (for Vt = Vto) vs. Radiation Dose
Gate Two Bias (V)
0
-1
-2
-3
-4
-5
-6
-7
-8
0
20
40
60
80
100
120
140
160
Radiation Dose (krad(Si))

Figure C.173.



Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V

Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V

Constants:
VS -Ch1 .0000V

Figure C.174.

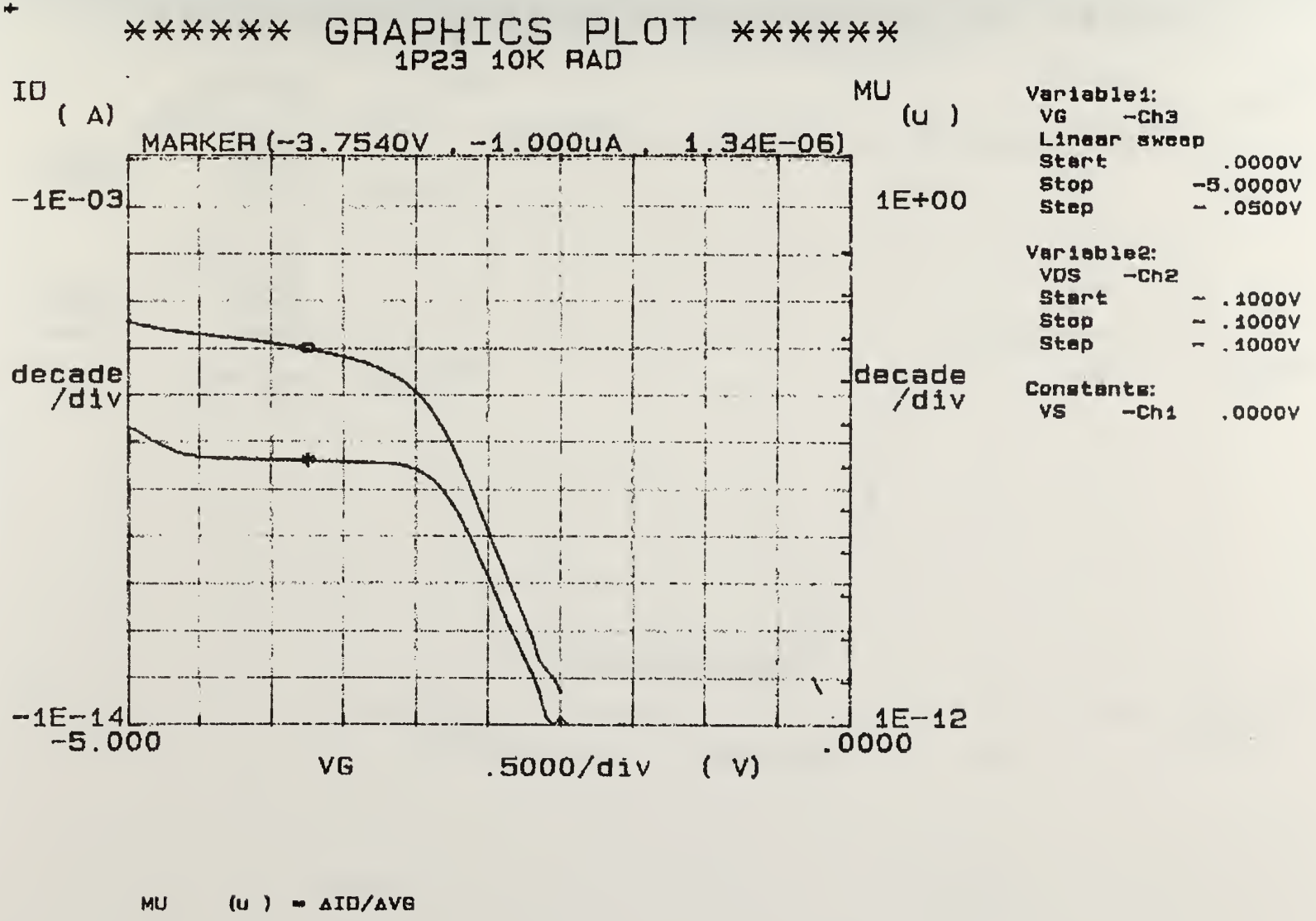

****** GRAPHICS PLOT ******
1P23 10K RAD
ID
(A)
MU
(u)
MARKER (-3.7540V , -1.000uA , 1.34E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-5.000
.0000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.175.

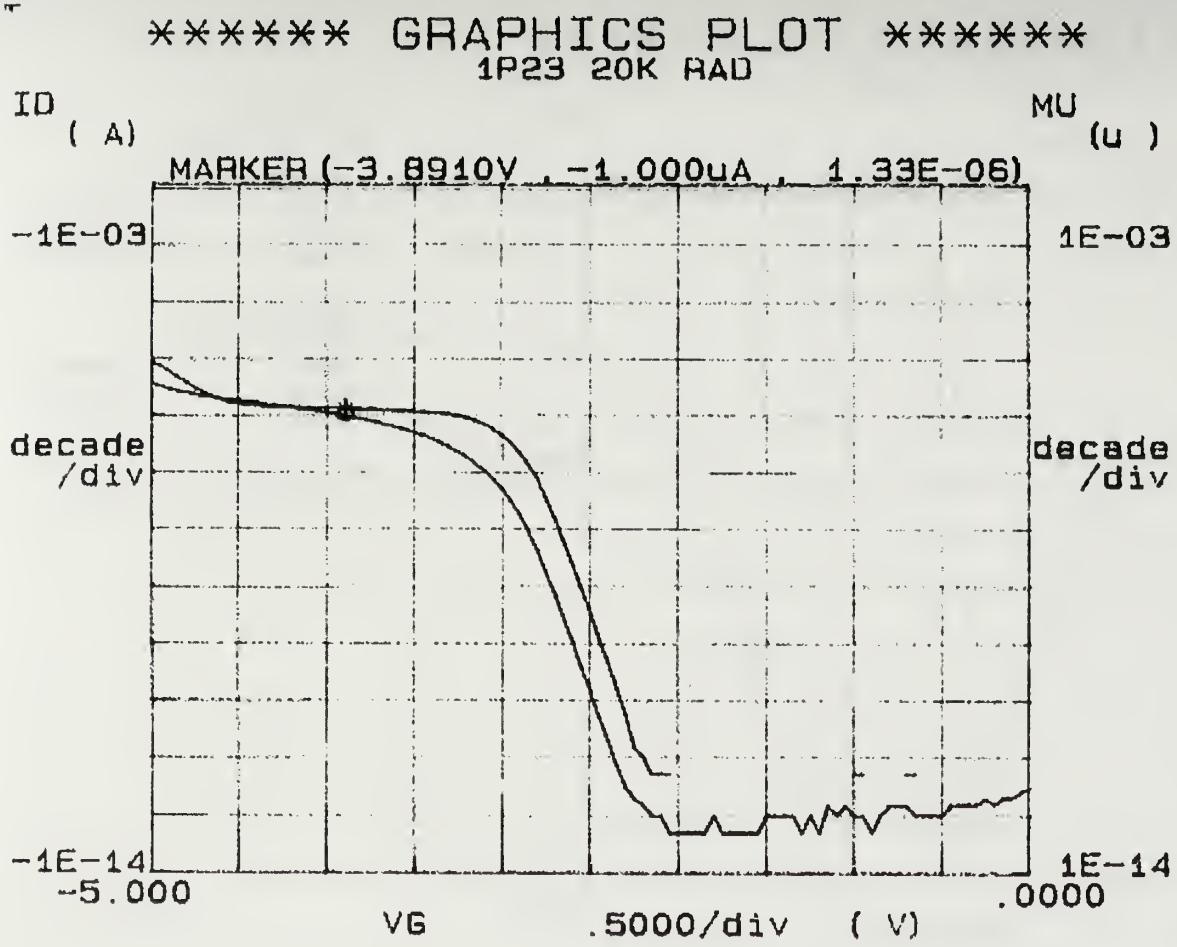

****** GRAPHICS PLOT ******
1P23 20K RAD
ID
(A)
MU
(u)
MARKER (-3.8910V , -1.000uA , 1.33E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-5.000
.0000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0500V
Variable2:
VDS -Ch2
Start -.1000V
Stop -.1000V
Step -.1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.176.

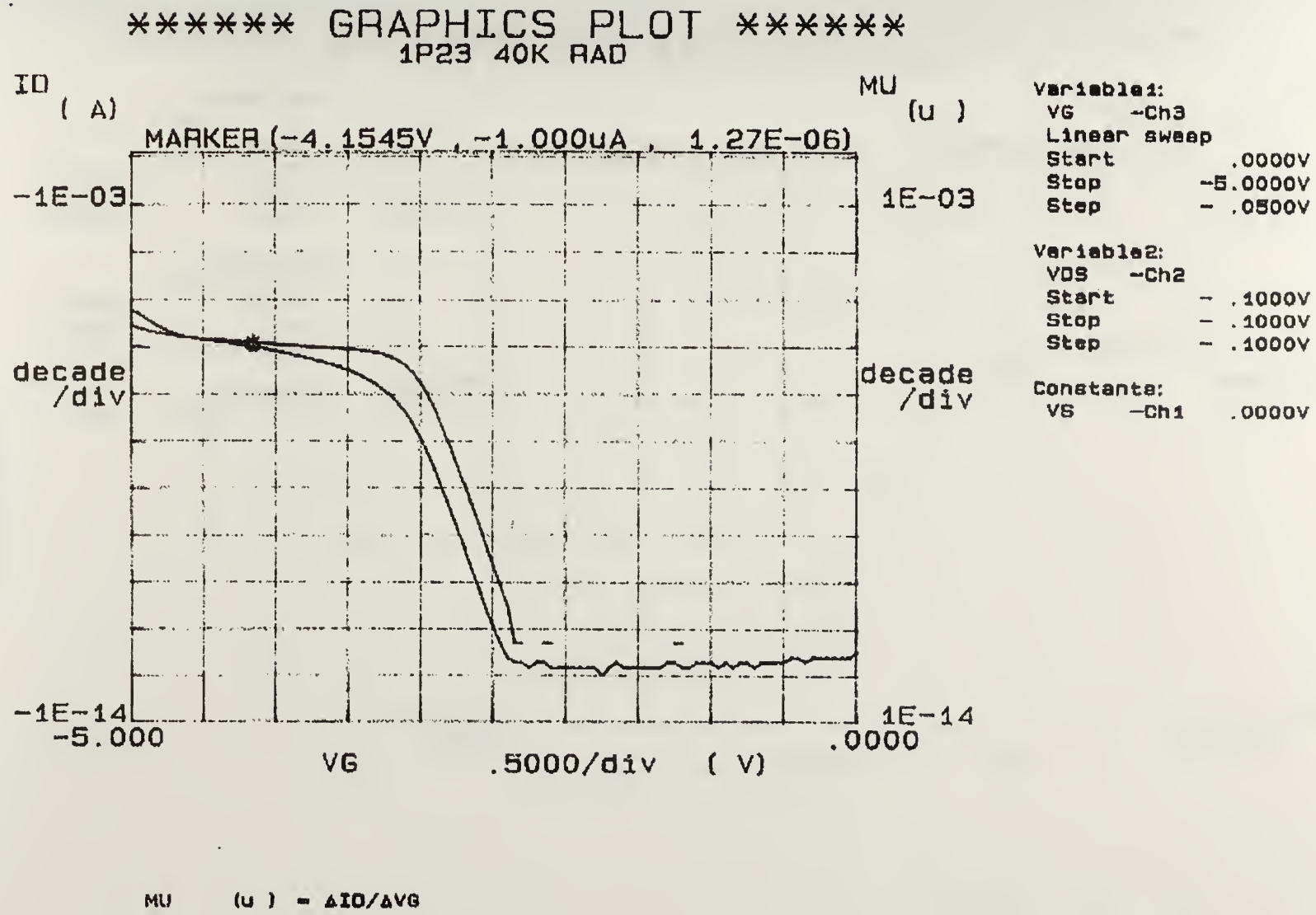

****** GRAPHICS PLOT ******
1P23 40K RAD
ID
(A)
MU
(u)
MARKER (-4.1545V , -1.000uA , 1.27E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-5.000
.0000
VG .5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constante:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.177.

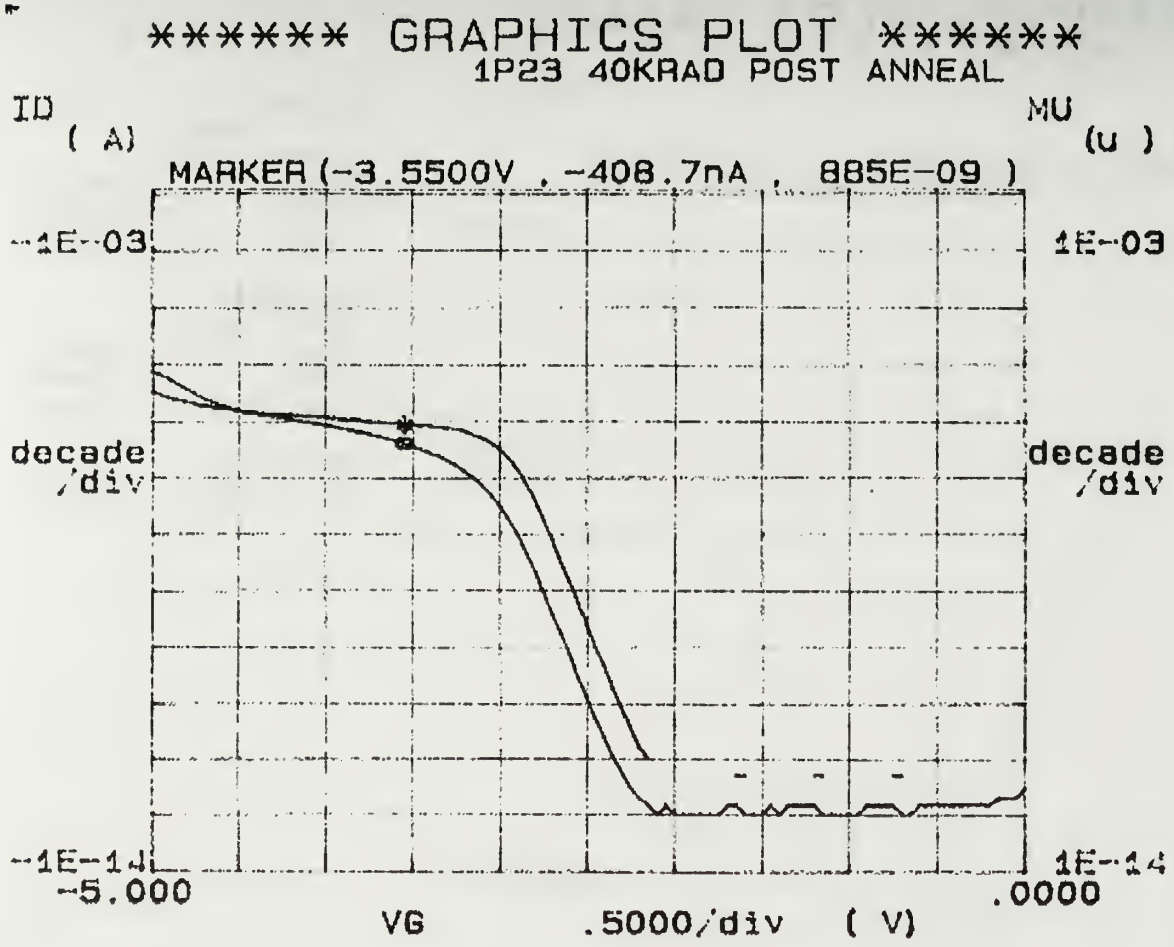

****** GRAPHICS PLOT ******
1P23 40KRAD POST ANNEAL
ID
(A)
MU
(u)
MARKER (-3.5500V , -408.7nA , 885E-09)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-5.000
.0000
VG .5000/div (V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0500V
Variable2:
VDS -Ch2
Start -.1000V
Stop -.1000V
Step -.1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.178.

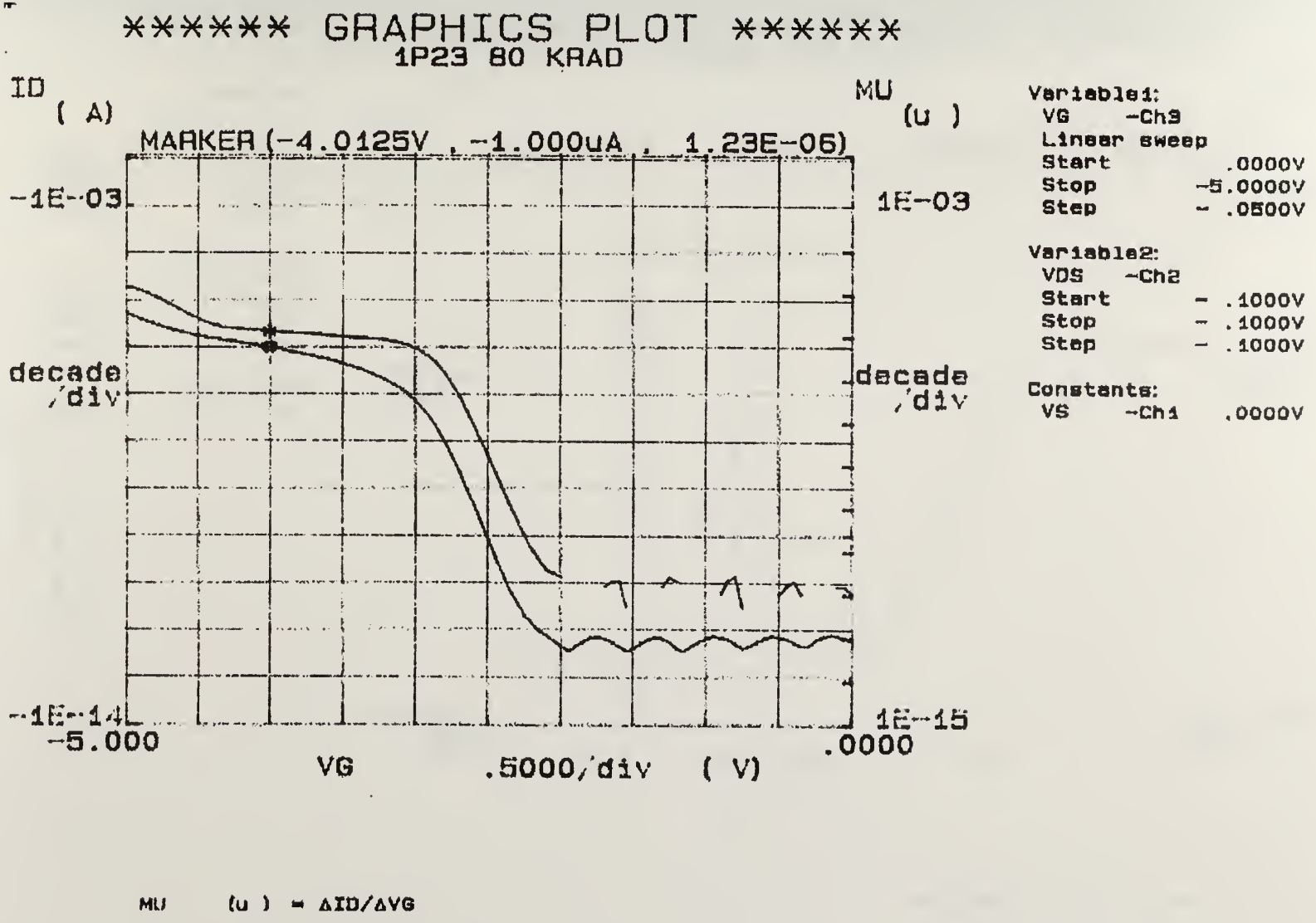

****** GRAPHICS PLOT ******
1P23 80 KRAD
ID
(A)
MU
(u)
MARKER (-4.0125V , -1.000uA , 1.23E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-15
-5.000
.0000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.179.

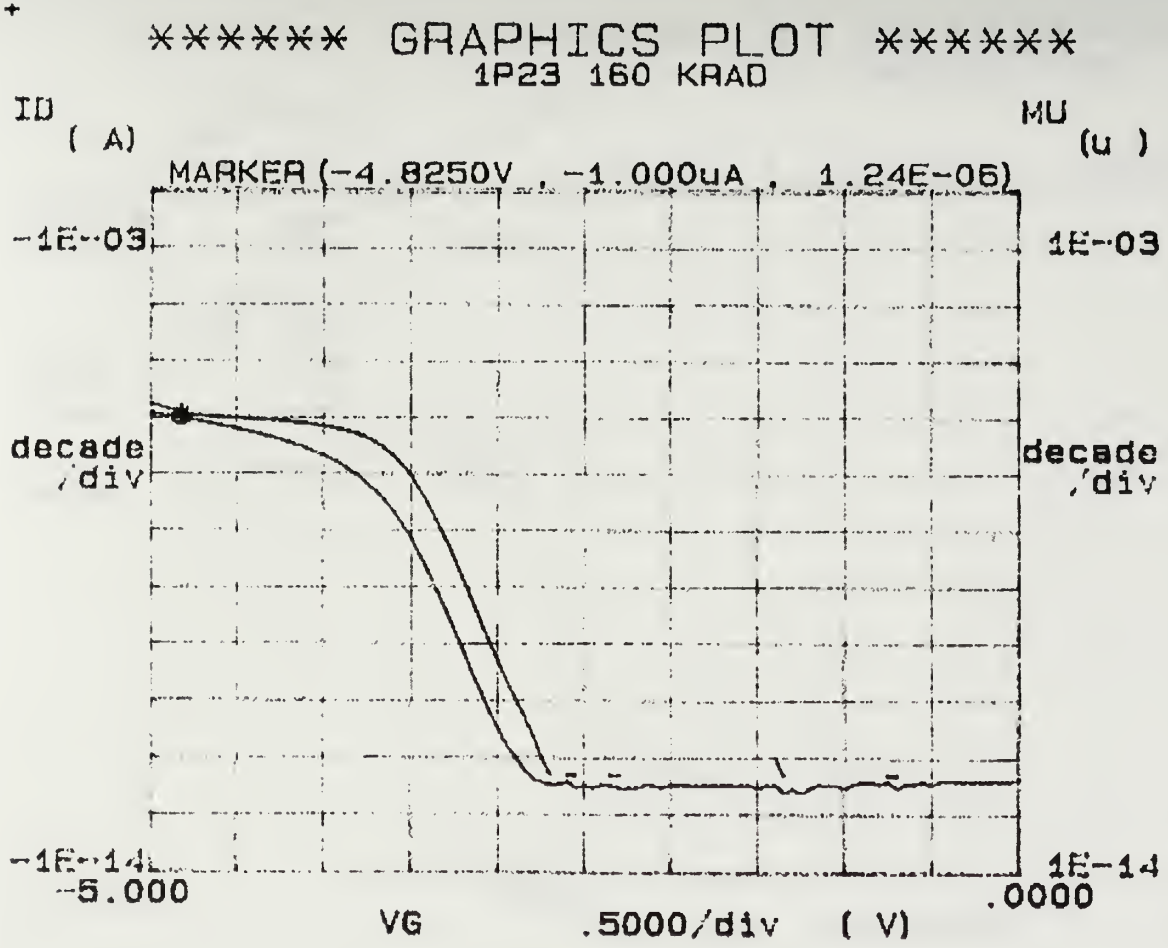

****** GRAPHICS PLOT ******
1P23 160 KRAD
ID
(A)
MU
(u)
MARKER (-4.8250V , -1.000uA , 1.24E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-5.000
.0000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VB -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.180.

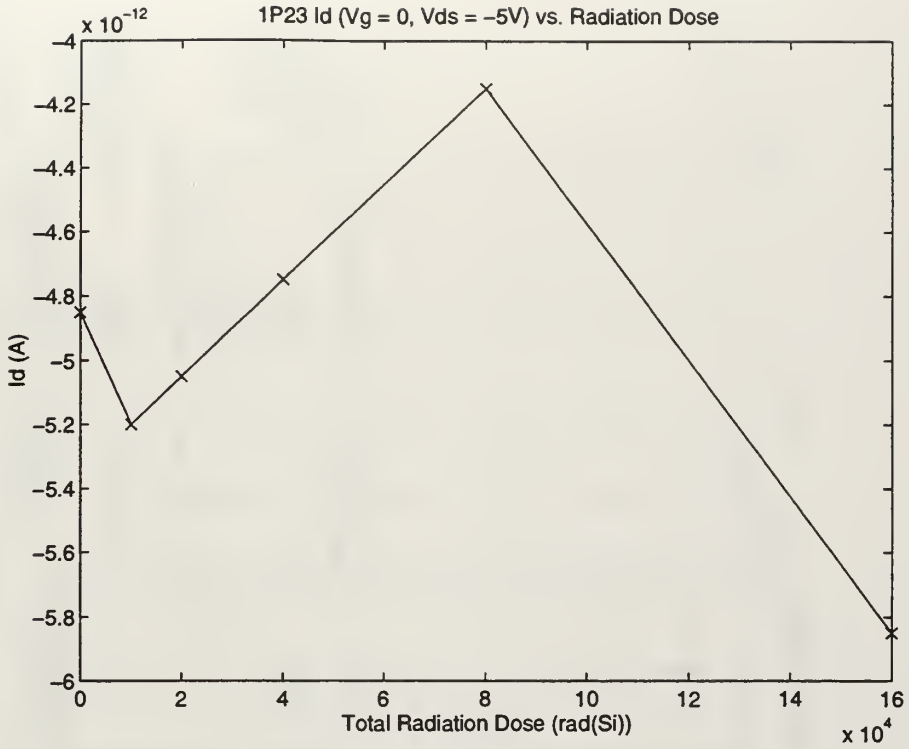


Figure C.181.

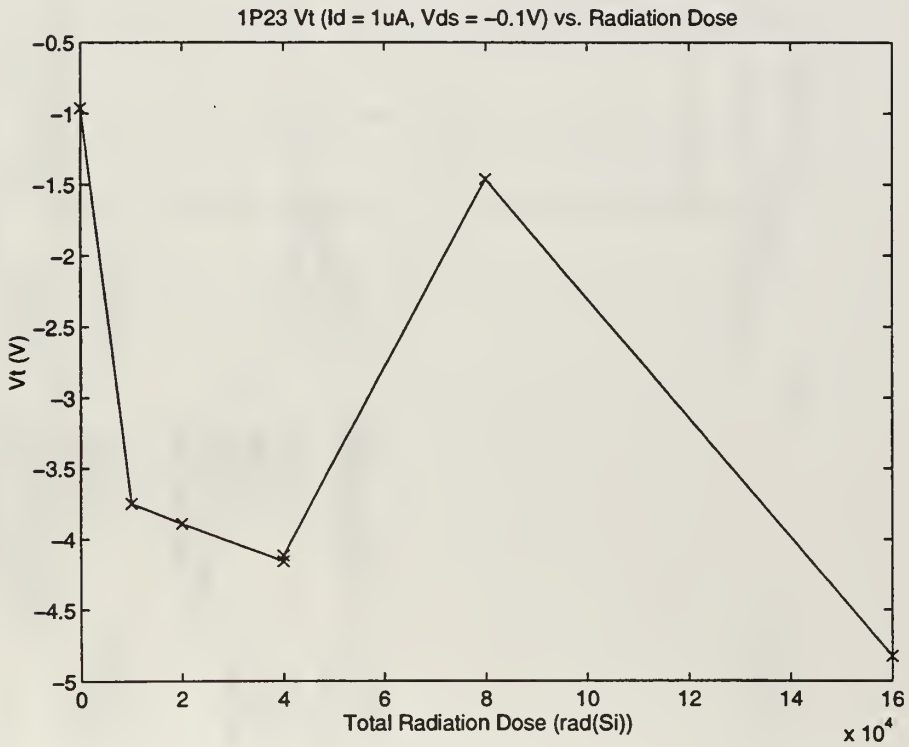


Figure C.182.

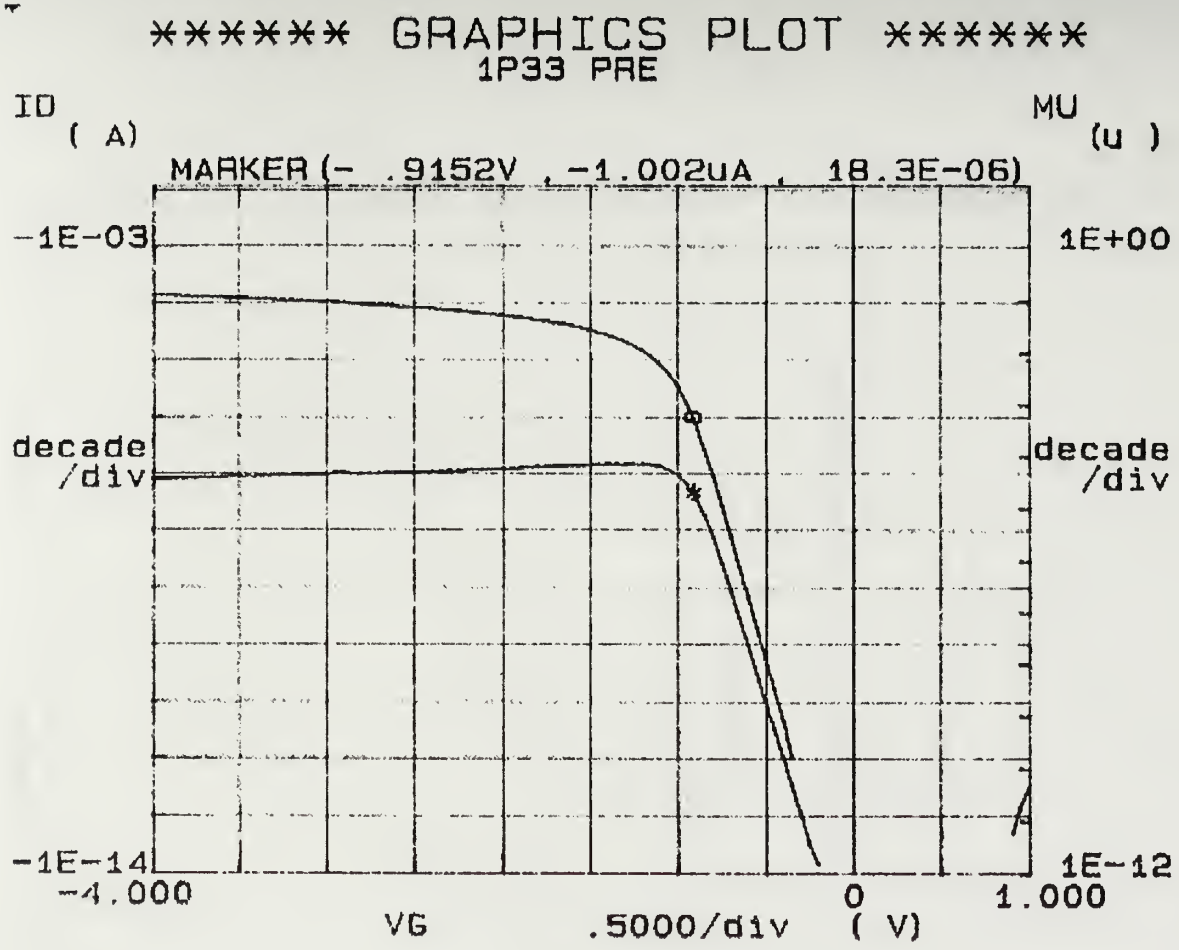

****** GRAPHICS PLOT ******
1P33 PRE
ID
(A)
MU
(u)
MARKER (- .9152V , -1.002uA , 18.3E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-4.000
0
1.000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.183.

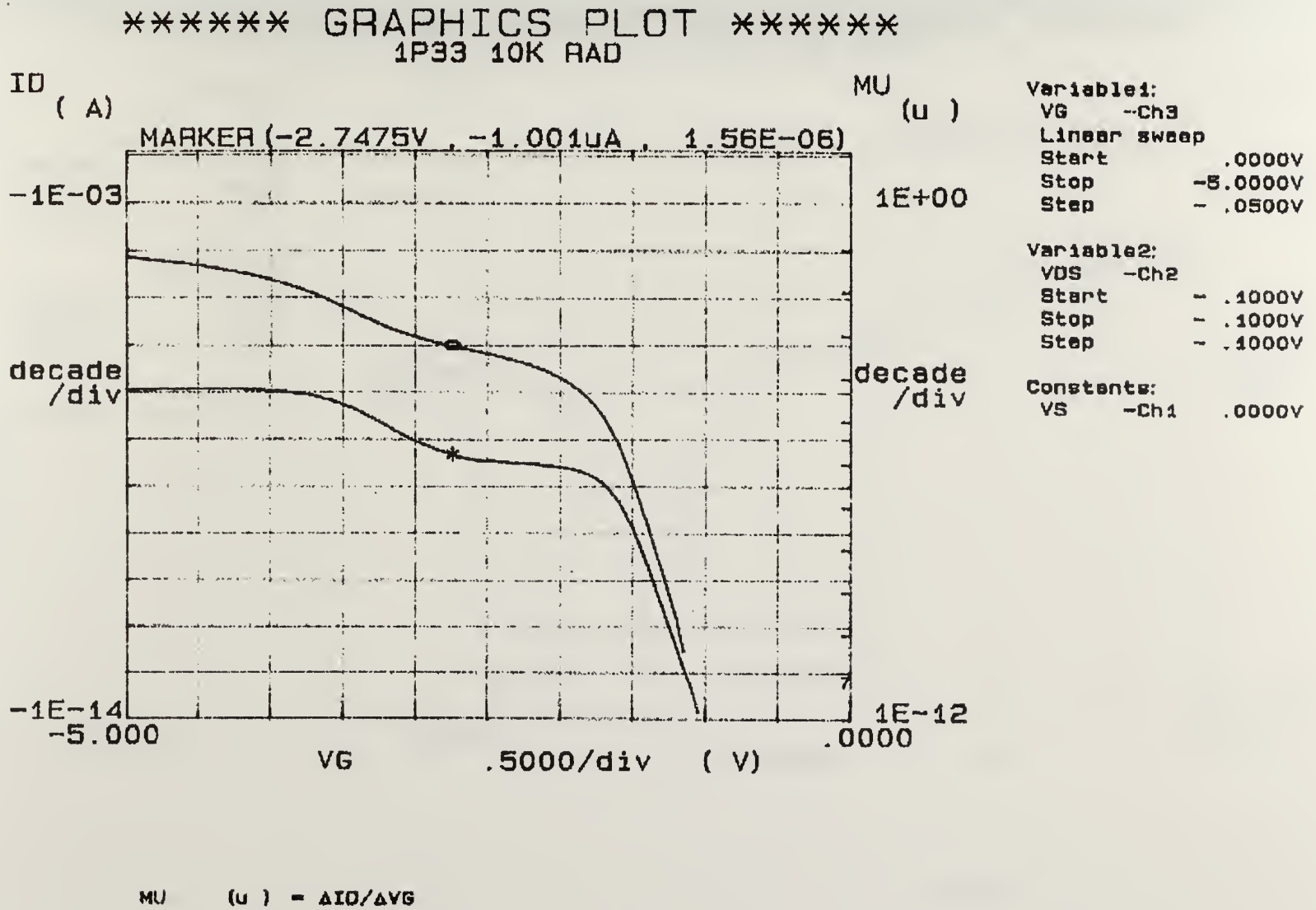

****** GRAPHICS PLOT ******
1P33 10K RAD
ID
(A)
MU
(u)
MARKER (-2.7475V , -1.001uA , 1.56E-06)
-1E-03
1E+00
decade
/div
decade
/div
-1E-14
1E-12
-5.000
.0000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.184.

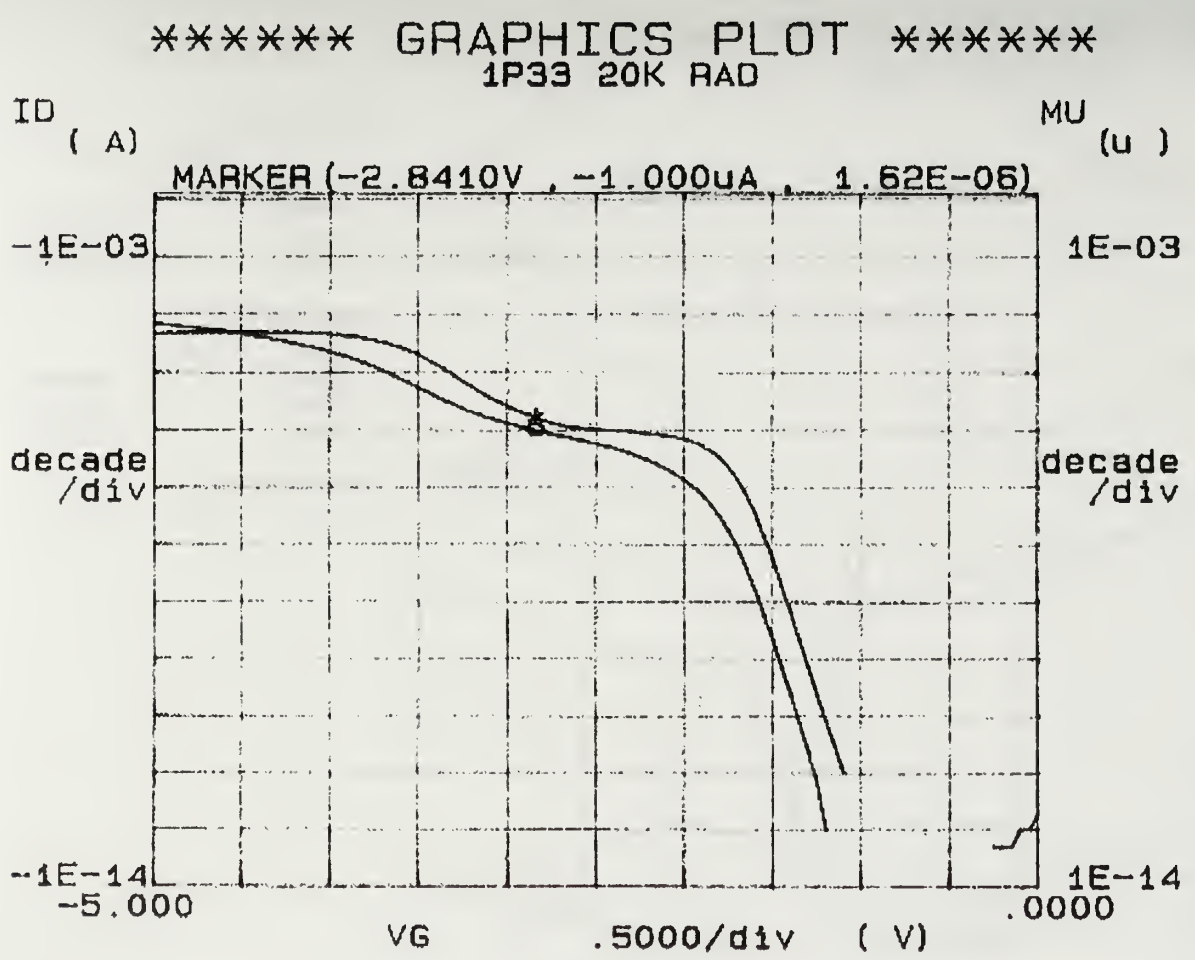

****** GRAPHICS PLOT ******
1P33 20K RAD
ID
(A)
MU
(u)
MARKER (-2.8410V , -1.000uA , 1.62E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-5.000
.0000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.185.

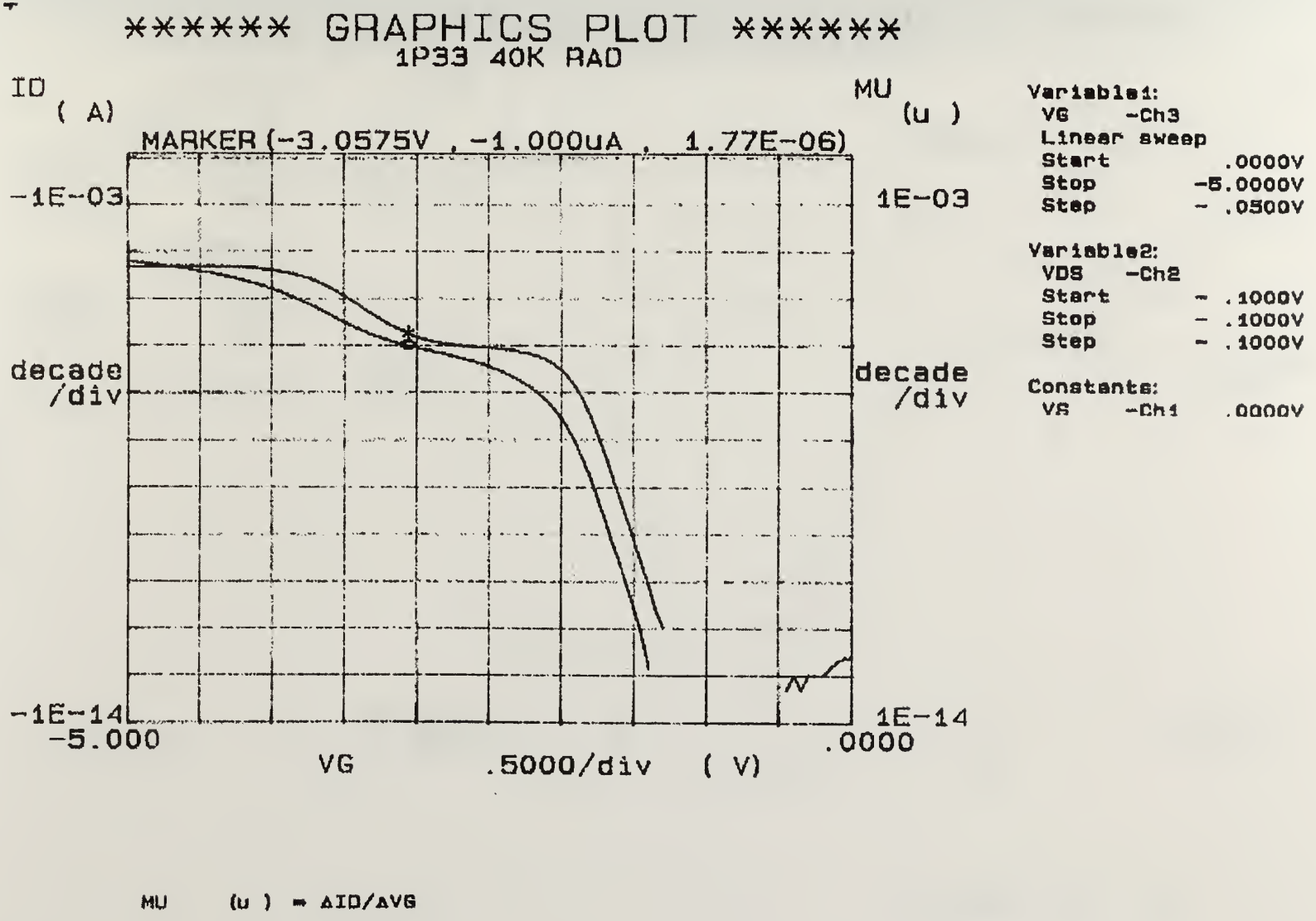
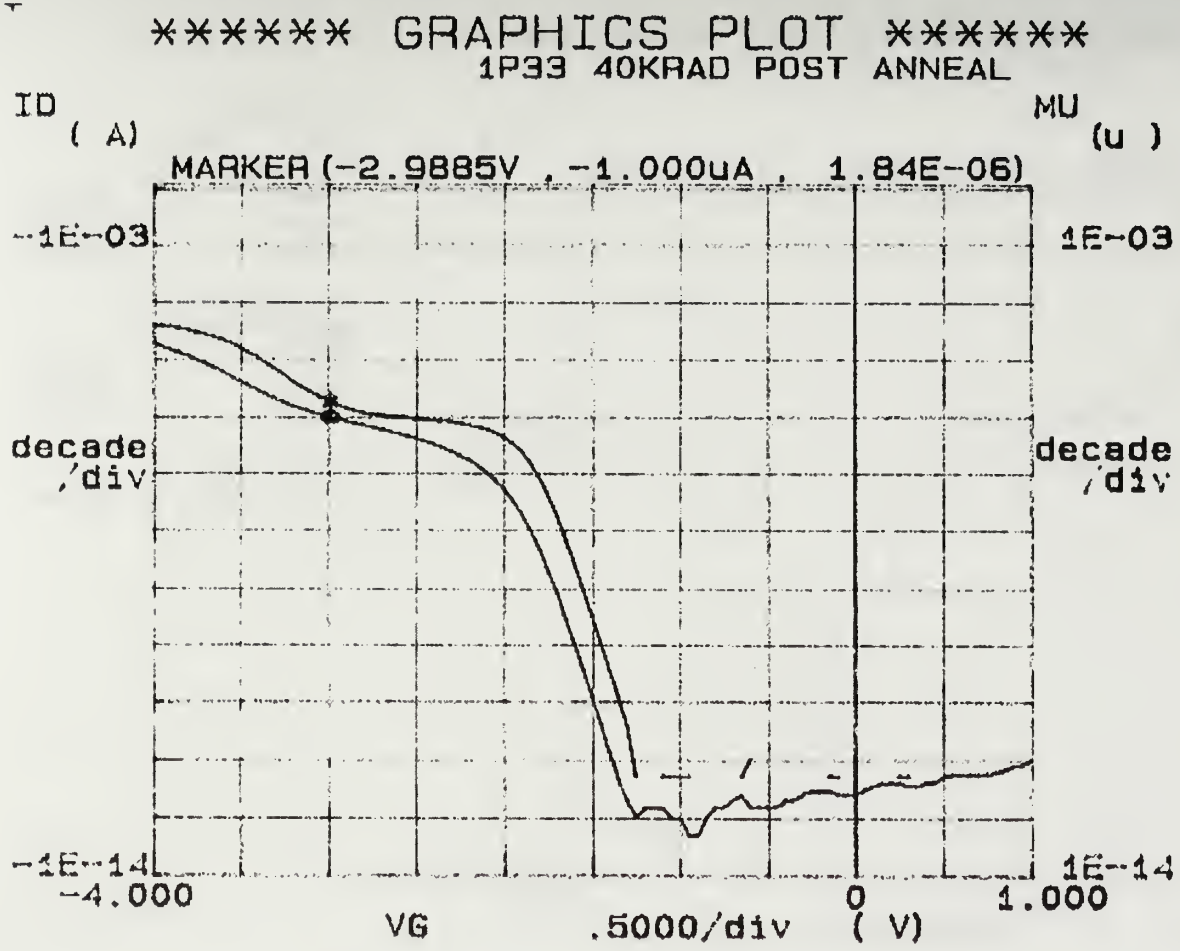

****** GRAPHICS PLOT ******
1P33 40K RAD
ID
(A)
MU
(u)
MARKER (-3.0575V , -1.000uA , 1.77E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-14
-5.000
.0000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.186.



Variable1:
VG -Ch3
Linear sweep
Start 1.0000V
Stop -4.0000V
Step - .0500V

Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V

Constants:
VS -Ch1 .0000V

Figure C.187.

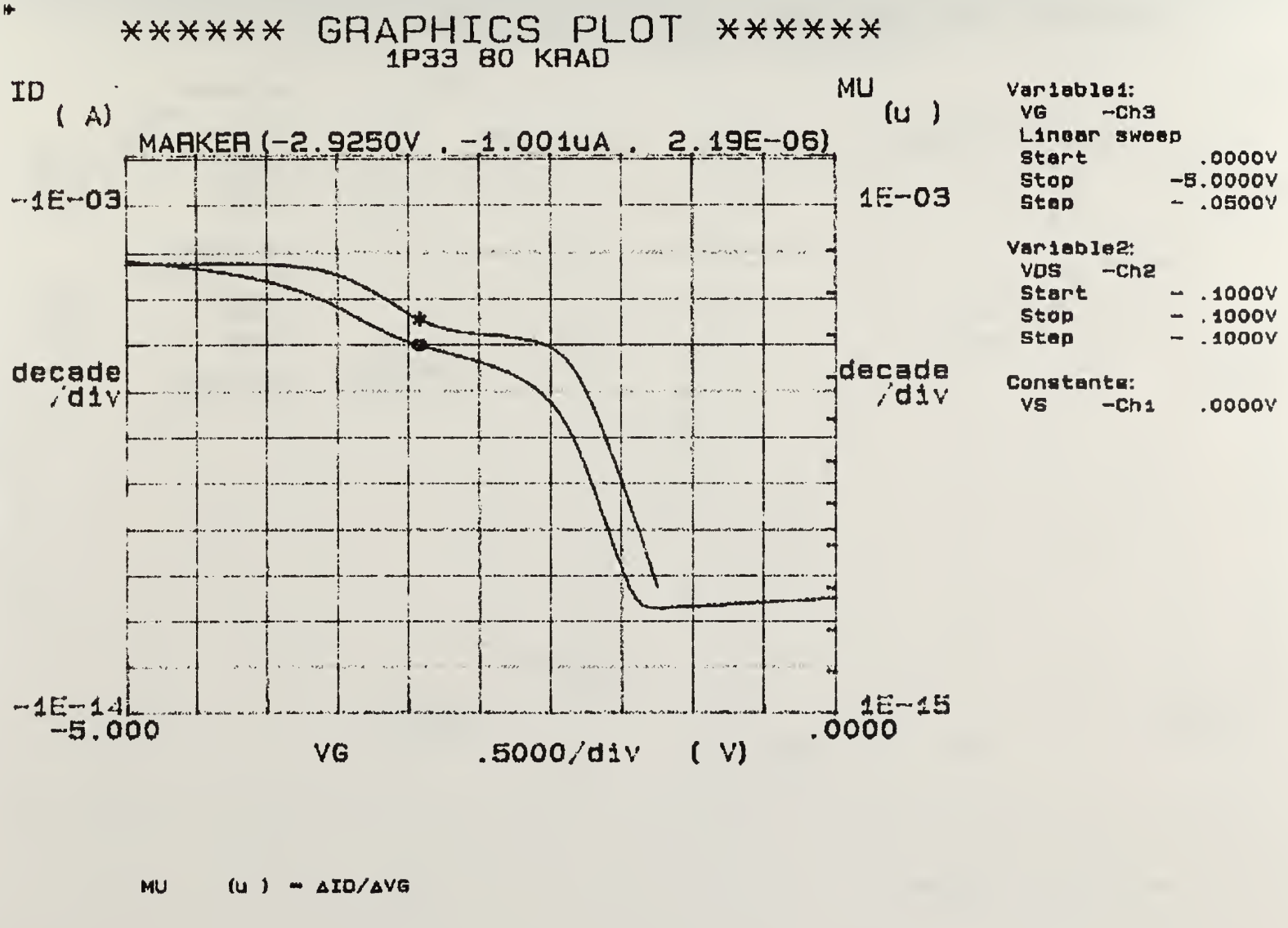
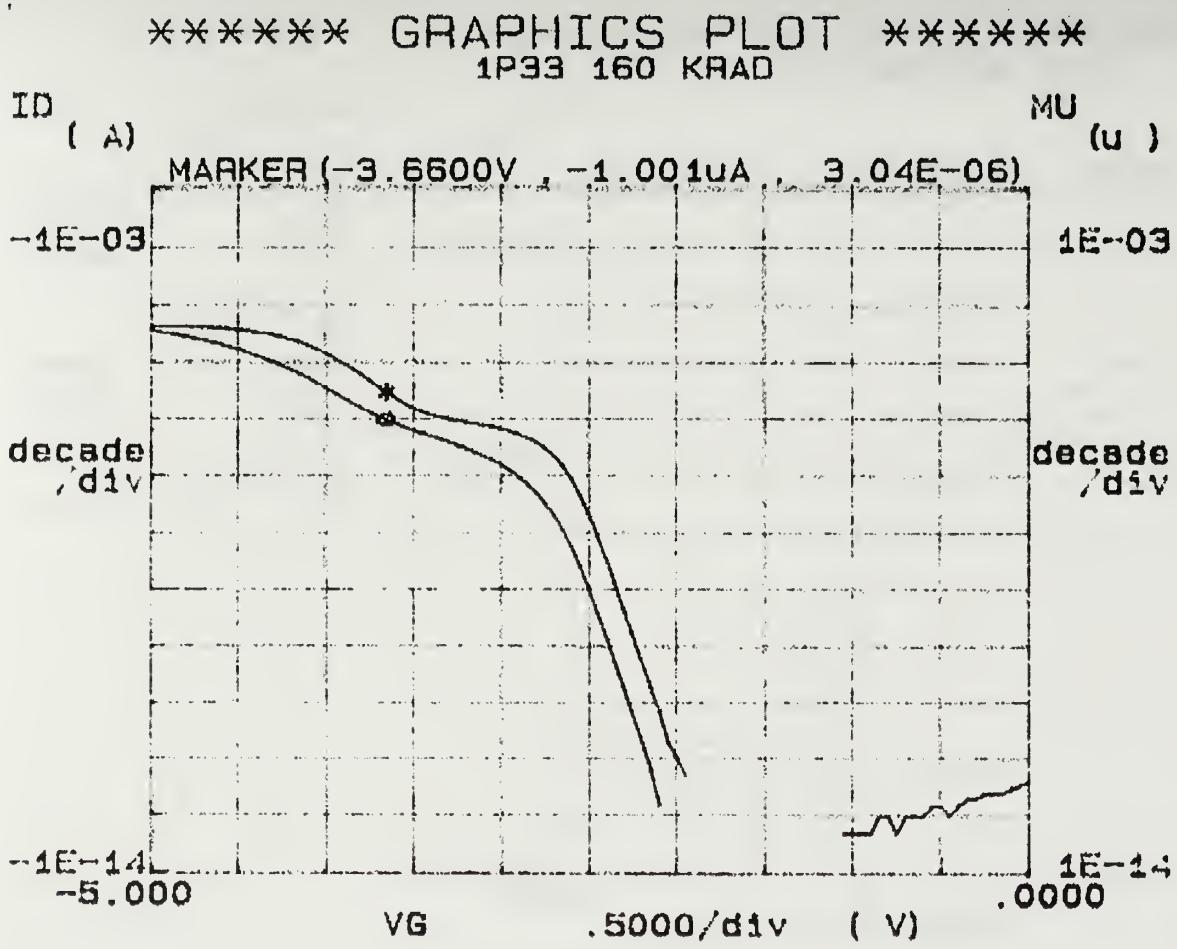

****** GRAPHICS PLOT ******
1P33 80 KRAD
ID
(A)
MU
(u)
MARKER (-2.9250V , -1.001uA , 2.19E-06)
-1E-03
1E-03
decade
/div
decade
/div
-1E-14
1E-15
-5.000
.0000
VG
.5000/div
(V)
Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .0500V
Variable2:
VDS -Ch2
Start - .1000V
Stop - .1000V
Step - .1000V
Constants:
VS -Ch1 .0000V
MU (u) = ΔID/ΔVG

Figure C.188.



Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0500V

Variable2:
VDS -Ch2
Start -.1000V
Stop -.1000V
Step -.1000V

Constants:
VB -Ch1 .0000V

Figure C.189.

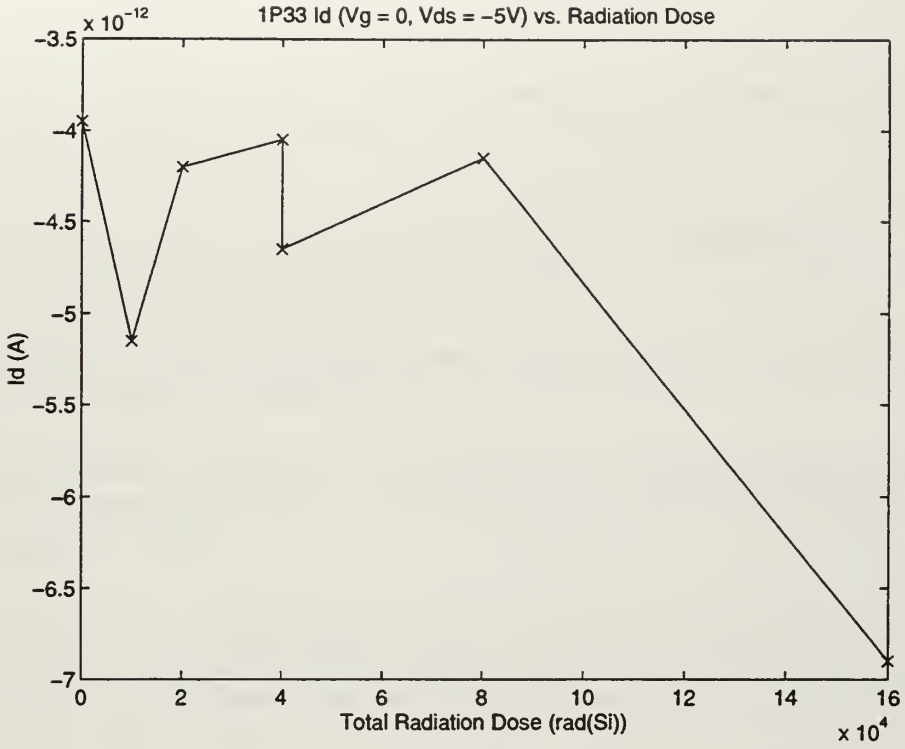


Figure C.190.

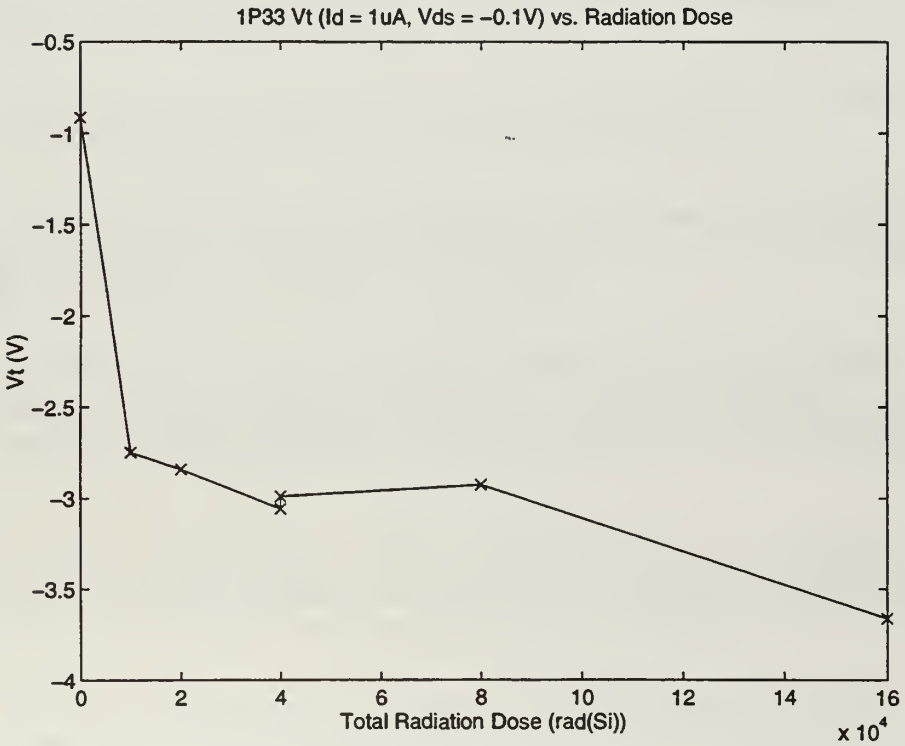


Figure C.191.

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